(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
3 October 2002 (03.10.2002)

PCT

(10) International Publication Number
WO 02/078059 A1

(51) International Patent Classification[7]: H01L 21/00

(21) International Application Number: PCT/US01/32572

(22) International Filing Date: 18 October 2001 (18.10.2001)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
09/813,859 22 March 2001 (22.03.2001) US

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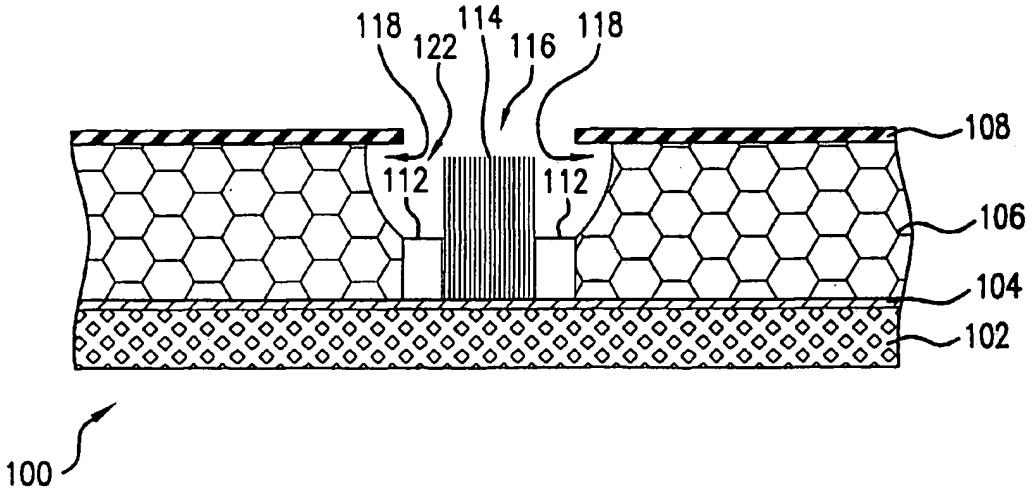
(81) Designated States *(national)*: AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DZ, EE, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, MZ, NO, NZ, PL, PT, RO, RU, SD, SE, SG, SI, SK, SL, TJ, TM, TR, TT, TZ, UA, UG, UZ, VN, YU, ZA, ZW.

(84) Designated States *(regional)*: ARIPO patent (GH, GM, KE, LS, MW, MZ, SD, SL, SZ, TZ, UG, ZW), Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European patent (AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE, TR), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

Published:
— *with international search report*

For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.

(54) Title: METHODS FOR MANUFACTURE OF SELF-ALIGNED INTEGRALLY GATED NANOFILAMENT FIELD EMITTER CELLS AND ARRAY



(57) Abstract: The present invention discloses a new field emitter cell (100) and array consisting of groups of nanofilaments (114) forming emitter cathodes. Control gates are microprocessed to be integrally formed with groups of nanofilament emitter cathodes on a substrate. Groups of nanofilaments are grown directly on the substrate material. As a result, the control gates and groups of nanofilaments are self-aligned with one another.

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METHODS FOR MANUFACTURE OF SELF-ALIGNED INTEGRALLY GATED NANOFILAMENT FIELD EMITTER CELL AND ARRAY

BACKGROUND OF THE INVENTION

Technical Field

The present invention relates to methods for manufacture of several distinct embodiments of a field emitter cell and array, in particular, to an integrally gated, self-aligned field emitter cell and array whose cathode is formed of a recently discovered class of materials of nanotubes and nanowires, collectively referred to as nanofilaments.

Background Art

Field emitters arrays (FEAs) are naturally small structures which provide reasonably high current densities at low voltages. Typically, FEAs are composed of emitter cells in the form of conical, pyramidal, or cusp-shaped point, edge or wedge-shaped vertical structures. Each cell is electrically insulated from a positively charged extraction gate and produces an electron beam that travels through an associated opening in the positively charged gate.

The typical field emitter structure includes a sharp point at the tip of the vertical structure (field emitter) and opposite an electrode. In order to generate electrons which are not collected at the extraction electrode, but can be manipulated and collected elsewhere, an aperture is created in the extraction electrode. The aperture is larger (e.g., two orders of magnitude) than the radius of curvature for the field emitter.

Consequently, the extraction electrode is a flat horizontal surface containing an extraction electrode aperture for the field emitter. Such an extraction electrode is referred to as the gate electrode. The field emitter is centered horizontally in the gate aperture and does not touch the gate although the vertical direction of the field emitter is perpendicular to the horizontal plane of the gate. The positive charges on the edge of the gate aperture surround the field emitter symmetrically so that the electric field produced between the field emitter and the gate causes the electrons to be emitted from the field emitter in a direction such that the electrons are collected on an electrode (anode) that is separate and distinct from the gate. The smaller the aperture (e.g., the closer the edge of the gate aperture is to the field emitter), the lower the voltage required to produce field emission of electrons.

The sharp point at the tip of the field emitter provides for reduction in the voltage necessary to produce field emission of electrons. As a result, numerous micro-manufacturing techniques have been developed to produce various sharp tip designs. Current techniques include wet etching, reactive ion etching (RIE), and a variety of field emitter tip deposition techniques.

Effective methods generally require the use of lithography which has a number of inherent disadvantages including a high equipment and manufacturing cost. For example, the high degree of spatial registration requires expensive high resolution lithography.

Additionally, cathode structures include very small localized vacuum electron sources which emit sufficiently high current. However, these vacuum electron sources are difficult to fabricate for practical applications. This is particularly true when the sources are required to operate at reasonably low voltages. Presently available thermionic sources do not emit high current densities, but rather result in small currents being generated from small areas. In addition, thermionic sources must be heated, and thus require special heating circuits and power supplies. Photoemitters have similar

problems with regard to low currents and current densities.

Recent advancements in nanotechnology have resulted in the creation of nanofilaments including nanotubes. One such example is carbon nanotubes. These nanotubes behave like metals or semiconductors and can conduct electricity better than copper, transmit heat better than diamond, and are among some of the strongest materials known while being only a few nanometers in diameter. Nanofilaments can have small diameters, ranging down to only a few nanometers. The nanofilaments may be grown to various lengths (e.g., 100-1000 nm) yet their diameter remains uniform. The aspect ratio (length to diameter) is extremely high.

Nanofilaments in the form of nanotubes have a hollow edge which is on the order of a couple of Angstroms thick. The nanotubes may be either single, double, or multiple walled (i.e., one nanotube within a second, third or further nanotube). For a more comprehensive discussion on carbon nanotubes, see "Carbon Nanotubes Roll On," Physics World, June 2000, pages 29-53.

Carbon nanotubes have been proposed as excellent candidates for use as field emitter cathodes due to: (1) the extreme sharpness of their edges and the extremely large aspect ratio, which enable the achievement of low operating voltages; (2) the resistance to tip blunting by residual back ion bombardment due to the uniform wall thickness throughout their height; (3) the relative inertness, high mechanical strength and current carrying capacity; and (4) an inherent current-limiting mechanism in the presence of adsorbed water which retards emitter burn out and destruction by arcing, a problem plaguing the present day FEAs. Nanotubes have been demonstrated in use as a cathode in a cathode lighting element in which the carbon-nanotubes act as the field-emitting cathode.

To be effective emitters, the nanofilaments need to be oriented largely perpendicular to the substrate. Recently, this property has been achieved by growing the nanofilaments on substrates under suitable conditions such as by high temperature chemical vapor deposition (CVD) on catalytic surfaces. For example, CVD has been used to form extremely vertical and uniformly grown carbon nanotubes directly above a metal catalyst substrate of patterned and oxidized iron patches. The resulting nanotubes form an ungated clump electrode which provides a stable field emission over the entire test duration of 20 hours.

On the other hand, high emission current from carbon nanotubes oriented parallel to the substrate has also been observed, which can be attributed to defects on the tube sidewalls. Nanotubes in this orientation can be expected to erode more quickly than those oriented perpendicular to the substrate by residual back ion bombardment.

However, these nanofilament electrodes are not gated and thus, have limited practical use as field emitters. In order to use nanofilaments as field emitters, one must control the operating characteristics of the nanofilaments, i.e., the turning on and off of small selected groups (i.e. clumps) of nanofilament emitters which comprise an array of emitter cells (e.g. pixels). This control is accomplished by providing a gate electrode, whose applied voltage bias controls the turning on, turning off and the field emission current magnitude. In order to enable low voltage operation, it is necessary to provide a control gate in very close proximity to a group of nanofilament emitters.

One proposed method of forming a gated nanofilament field emitter includes pre-positioning a paste layer of the nanotubes separately on a substrate and assembling a control grid gate assembly to the paste layer of nanofilaments. This and other presently available manufacturing techniques (all non-integral) fail to provide practical (e.g., in terms of functional and economical) gating of nanofilaments, e.g., nanotube, field emitters.

One clear disadvantage of this method is that the resulting gated unit tends to be large when

compared to integrally formed conventional field emitter cells, which limits the resolution. As a result of the increased emitter-grid gate separation, these grid-gated emitters require a much higher gate voltage (hundreds of volts as compared to tens of volts for integrally gated emitters) for their operation.

An additional disadvantage with presently available carbon nanotube field emitting cathodes is that the grid-type control gates and nanotube cathodes are not self-aligned with one another because the control grid gate is assembled to the nanotubes after a paste layer of nanotubes has already been formed. As a result, the gate current (e.g., current intercepted by the gate) tends to be very high which can cause overheating. In addition, this approach generally does not provide precise control and operation of the FEA and in particular, precise control of individual cells forming the emitter array, as compared to integrally formed and self-aligned control gate and cathode design.

DISCLOSURE OF THE INVENTION

The present invention reveals methods for manufacture of several distinct embodiments of a self-aligned, integrally gated nanofilament field emitter cell and array wherein a nanofilament cathode (in the form of a group or "clump" of nanofilaments) and control gate are formed through the microprocessing techniques of the subject invention, thereby self-aligning the nanofilament cathode with the control gate.

According to one aspect of the invention, a method for manufacture is provided for a field emitter cell which comprises an electrically conductive substrate layer. An insulator layer is disposed directly upon the substrate layer and an electrically conductive gate layer is disposed directly on the insulator layer. An aperture on the gate layer extends through the insulator layer to the substrate layer. A catalyst layer is applied to a surface conductively associated with the substrate layer. Electrically conductive nanofilaments are grown on the catalyst layer. The group of nanofilaments is electrically isolated from the gate. When the field emitter cell is operational, the group of nanofilaments acts as a cathode.

In alternate embodiments, the catalyst layer upon which the nanofilaments are grown is applied to top surfaces of various structures which comprise a post structure, a tip structure, and an obelisk structure extending from the substrate surface.

The invention, in another aspect thereof, concerns a method of manufacturing a field emitter cell comprising depositing an insulator layer on an electrically conductive substrate layer. A gate layer is formed on the insulator layer. An aperture, with a larger dimension in the gate layer than in the insulator layer, extends downward through the insulator layer to the substrate layer. A catalyst layer is applied to a surface conductively associated with the substrate layer. Electrically conductive nanofilaments are grown on the catalyst layer.

In accordance with yet another aspect of the invention, there is provided a method of manufacturing a field emitter cell comprising applying a catalyst layer to a portion of an electrically conductive substrate layer. An insulator layer is deposited on the catalyst layer. A gate layer is formed on the insulator layer. An aperture is formed in the gate layer, extending through the insulator layer to the catalyst layer. Nanofilaments are then grown on the catalyst layer.

One advantage of the present invention is that a method of manufacture for a field emitter cell is provided in which the cathode comprising a group of nanofilament emitters in close proximity to a control gate. As a result of this close proximity, in conjunction with the extreme nanofilament tip sharpness, the control gate uses a much lower emitter operating voltage as compared with currently demonstrated nanofilament grid-gate or ungated field emitter designs.

Yet, another advantage of the present invention is the resistance of the nanofilaments to blunting by residual back ion bombardment because the edge will remain at the same sharpness due to the uniform thickness throughout their heights.

Yet, another advantage of the present invention is that the carbon nanotube has a relatively clean and inert surface (i.e. no non-volatile oxides), which enhances higher emission stability. Another advantage is that often these nanofilaments either possess or can be tailored to posses sufficient resistance which, during emission, will lead to an IR (current times resistance, from the equation V = IR where V = voltage, I = current, and R = resistance) drop in the potential between the gate and the emitter, thereby preventing emitter burn-out by limiting the current. Due to their small bulk, the properties of nanofilaments, especially resistivity, can be readily and profoundly altered by their adsorbing another material, doping, alloying, or formation of compounds, even to small extents. Further, carbon nanotubes, in the presence of adsorbed water, provide an inherent current-limiting mechanism which tends to retard emitter burn-out as disclosed in "Current Saturation Mechanisms In Carbon Nanotube Field Emitters," Applied Physics Letters, volume 76, no. 3, Kenneth A. Dean and Babu R. Chalamala, January 17, 2000.

It is an object of the present invention to provide methods for manufacturing a self-aligned integrally gated nanofilament field emitter cell and array.

It is another object of the present invention to provide methods for manufacturing a field emitter cell and array in which the gate electrode is placed in very close proximity to a group of nanofilament emitters.

It is yet another objective of the present invention to provide methods for manufacturing a field emitter cell and array in which the cathode is resistant to blunting and surface contamination.

It is yet another object of the present invention to provide methods for manufacturing a field emitter cell and array with a very low turn-on voltage and that has a stable field emission.

It is yet another object of the present invention to provide methods for manufacturing a field emitter cell and array that is very economical to manufacture because no precise lithography is required. In fact, no lithography is required in making this field emitter cell and array, if a stamping technology is used to make the masks for the etching of the starting apertures.

Further features and advantages of the present invention are set forth in, or apparent from, the description of preferred embodiments which follows.

BRIEF DESCRIPTION OF DRAWINGS

Figures 1(a)-1(g) illustratively depict the processing steps involved in fabricating a field emitter cell according to a first embodiment of the present invention;

Figures 2(a)-2(g) illustratively depict the processing steps involved in fabricating a field emitter cell according to a second embodiment of the present invention;

Figures 3(a)-3(g) illustratively depict the processing steps involved in fabricating a field emitter cell according to a third embodiment of the present invention in which the emitter cathode comprises a group of nanofilaments formed on a post structure;

Figures 4(a)-4(i) illustratively depict the steps involved in fabricating the field emitter cell according to a fourth embodiment of the present invention in which the emitter cathode comprises a group of nanofilaments formed on a post structure;

Figures 5(a)-5(d) illustratively depict the processing steps in fabricating a field emitter cell according to a fifth embodiment of the present invention in which the emitter cathode is formed as a group of nanofilaments on a conical tip or a tip-on-post emitter structure;

Figure 5(e) is a plot of the resulting field emission data of the fifth embodiment; and

Figure 6(a) illustratively depicts a sixth embodiment of a field emitter cell using a group of nanofilaments as the emitter cathode with an offset control gate according to the present invention, and Figure 6(b) is a plot of the field emission data of the sixth embodiment.

Figures 7(a) and 7(b) illustratively depict certain stages of the processing steps involved in fabricating a field emitter cell according to the seventh embodiment of the present invention.

Figures 8(a) through 8(d) illustratively depict certain stages of the processing steps involved in fabricating a field emitter cell according to the eighth embodiment of the present invention.

BEST MODES FOR CARRYING OUT THE INVENTION

1st Embodiment

Referring now to Figures 1(a)-1(g), illustratively depicted therein are the steps of fabricating a field emitter cell 100 according to the first embodiment of the present invention. The field emitter cell 100 is formed on a conductive or semiconductive substrate layer 102. Optimally, substrate layer 102 is a porous silicon substrate with a nanoporous layer in order to provide for highly directional nanotube growth.

A catalyst layer 104 is deposited on substrate layer 102 by sputtering or evaporative deposition of a suitable catalyst material. The catalyst layer promotes the growth of nanofilaments of interest under appropriate growth conditions (described below). For carbon nanotube growth, the most effective catalyst layer may comprise iron, nickel or cobalt.

Optionally, at this point, the catalyst-coated substrate may be annealed in air to anneal and oxidize the catalyst layer 104. Alternatively, the annealing/oxidation of catalyst layer 104 may be done later or it may be left unoxidized. Insulator layer 106, composed of SiO_2 or other suitable insulator material, is deposited to a few thousand Angstroms thick.

Gate layer 108 is then deposited on insulator layer 106. Gate layer 108 is composed of either a semiconducting material, a metal, or a multiple layer conductive material that does not catalyze nanofilament growth. For example, the material of gate layer 108 may comprise two layers including a chromium layer on a p-type polysilicon layer deposited over the insulator layer 106.

Gate aperture 110 is formed by patterning and etching using any of a number of techniques known in the art such as the one described in the commonly-owned U.S. Patent No. 6,084,245. For example, circular posts of resist (not shown) are patterned and fabricated on the gate layer 108 followed by evaporation deposition of a thin chromium layer and then lift-off of the resist post to leave patterned circular apertures in the chromium layer (not shown). Using the chromium layer as an etch mask, standard reactive ion etching (RIE) is used to anisotropically etch aperture 110 through gate layer 108 and insulator layer 106, terminating on the catalyst layer 104.

Referring now to Figure 1(b), preferably a CVD method is used to deposit a conformal, stand-off layer 112 on the horizontal surfaces 109 of gate layer 108 and along the vertical sides of gate layer 108 and insulator layer 106 and the horizontal surface of catalyst layer 104 exposed during the etching of aperture 110. The thickness of stand-off layer 112 is adjusted to reduce the diameter of aperture 110. Referring now to Figure 1(c), standard anisotropic RIE of the stand-off layer is carried out to remove the stand-off layer 112 disposed on the horizontal surface 109 of gate layer 108. In addition, RIE removes stand-off layer 112 deposited at the bottom of aperture 110, thereby exposing catalyst layer 104.

If catalyst layer 104 was not previously annealed and oxidized prior to stand-off layer 112 deposition, cell structure 100 is optionally annealed in air at a temperature to substantially oxidize th

exposed catalyst layer 104 as previously described.

Referring now to Figure 1(d), nanofilaments are grown on top of the exposed catalyst layer 104 disposed at the bottom of gate aperture 110. Nanofilaments 114 are pr ferably grown perpendicular to the exposed catalyst surface 104 using growth conditions known in the art, such as those described in connection with the method discussed in Science, Vol. 283, 512 (1999) by S. Fan et al.

Nanofilaments 114, composed of carbon nanotubes, initiate growth on the iron/iron oxide particles that form catalyst layer 104. Optimally, the nanofilaments 114 are grown to the level of gate layer 108 or slightly below, although they may also be at a higher level than the gate layer 108.

Nanofilaments 114, composed of carbon nanotubes, should be grown under conditions that do not form non-nanofilament carbonaceous material on surfaces that do not contain a catalyst. For example, a low hydrocarbon-to-reducing gas ratio should be used in a CVD method.

If needed, cleaning/clearing debris from the top surfaces of field emitter cell 100 such as horizontal surfaces 109 and the horizontal surface 113 of stand-off layer 112, may be accomplished by first filling gate aperture 110 with a protective layer such as a resist or silicon dioxide, followed by perpendicular RIE using oxygen to remove any carbonaceous layer and to etch away the top surface until the residual debris layer is removed.

Referring now to Figure 1(e), field emitter cell 100 is optionally dipped in a buffered hydrofluoric (HF) solution to remove the upper portion of stand-off layer 112. The hydrofluoric acid removes a portion of the stand-off layer 112 along with cutting into (i.e., removing) a portion of insulator layer 106 adjacent nanofilament clump electrode 116 in areas 118. The hydrofluoric acid is removed by gentle rinsing or weak sonication in distilled water.

Optimally, residual water in the cells is removed through a process of freeze-drying. During the freeze-drying, residual water is removed by sublimation. The freeze-drying minimizes the sticking of the individual nanofilaments 114 to the sidewall(s) of the aperture after a wet treatment. An alternative method of drying is by critical point drying, a technique commonly used to preserve mechanical integrity of biological specimen, in which the water is first replaced with a solvent which is then replaced with a liquefied gas (e.g., carbon dioxide). Minimum distortion occurs upon vaporization of the liquefied gas.

A portion of unanchored or weakly anchored nanofilaments 114 may be dislodged during the hydrofluoric acid and water rinse. Mechanical and electrical anchoring of the remaining attached nanofilaments to the cell structure 100, can be enhanced by plating with nickel at the base where the nanofilaments 114 meet catalyst layer 104.

Referring now to Figure 1(f), if nickel plating is desired, a sufficiently long hydrofluoric acid dip/rinse is first conducted to remove stand-off layer 112 from within aperture 110, thereby exposing catalyst layer 104. Subsequently, nickel 120 is plated up from the freshly exposed portions of the catalytic layer 104 at the bottom of aperture 110.

An alternative to the afore-mentioned HF treatment to remove the top portion of the stand-off layer 112 is by dry etching such as reactive ion etching, thereby avoiding any potential problem concerning nanofilaments sticking to the sidewalls of the aperture after a wet treatment.

Referring now to Figure 1(g), along with Figures 1(e) and 1(f), the resulting field emitter 100 has a gate layer 108 with a circular gate aperture 110. Clump electrode 116 forms the emitter portion consisting of a group of nanofilaments 114 with circular symmetry centered within gate aperture 110. Vacuum gap 122 is disposed between the top portion of clump cathode 116, insulator layer 106, and the edge of the gate aperture 110, electrically isolating the nanofilament emitters from the gate.

Electrical contact is established between the clump cathode 116, substrate 102, and any layers there between.

Operation of field emitter cell 100 involves the application of a positive voltage bias to the gate layer 108 relative to the clump cathode 116 to extract field emission of electrons from the clump cathode 116. Electrons may be collected on an anode (not shown) placed at a distance above the field emitter array device 100.

Many modifications may be made to this first embodiment to accommodate various manufacturing processes and operating conditions. For example, although nanofilaments 114 are composed of carbon nanotubes, alternate nanofilaments may be nanowires composed of Si, Ge, SiC, GaAs, GaP, InAs, InP, ZnS, ZnSe, CdS, CdSe, MoS_2, WS_2, and combinations thereof grown under appropriate growth conditions known in the art.

In addition, although clump cathode 116 is formed as a circular group of nanofilaments 114, other geometrical shape may be substituted, such as but not limited to, linear, square, and rectangular (not shown) by making appropriately modifications to the method described above. As is obvious to one of ordinary skill in the art, the placement and shape of the starting template structures (e.g. aperture) on the substrate determines the location and shape of resulting emitter cathodes, cells, and array.

2nd Embodiment

Figure 2(a)-2(g) illustratively depict a second embodiment which differs from the first embodiment in that in the second embodiment, catalyst layer 204 is deposited after gate layer 208 and stand-off layer 212 are deposited and etched. Therefore, the various processing steps of the second embodiment are the same as in the first embodiment unless otherwise noted.

Insulator layer 206 is deposited directly on substrate layer 202 by any suitable manner known in the art. Subsequently, gate layer 208 is formed on insulator layer 206, and gate aperture 210 is patterned and etched. Stand-off layer 212 is deposited along the surface of cell structure 200 which includes along the gate layer horizontal surface 209, the vertical wall surfaces within gate aperture 210 and along surface 203 of substrate 202 exposed during the etching of gate aperture 210 (Figure 2(b)). Next, stand-off layer 212 is removed from the horizontal surfaces of cell structure 200, namely gate layer horizontal surface 209 and substrate surface 203, using an anisotropic reactive ion etching (RIE) process (Figure 2(c)).

Catalyst layer 204 is directionally deposited along surface 203 and, unavoidably, along the horizontal surface 209 of gate layer 208. In addition, some catalyst material may be residually deposited along the vertical wall surfaces within gate aperture 210 (Figure 2(d)). Catalyst layer 204 may be composed of the same material as in the first embodiment. Optimally, the material of gate layer 208 passivates the material of catalyst layer - that is, under the nanofilament growth conditions, the catalyst layer on such a gate material no longer catalyze growth of nanofilaments. However, it is not necessary for the material of gate layer 208 to passivate the catalyst in this 2nd embodiment.

Catalyst material deposited on gate layer 208 and the top portion of the vertical side wall of stand-off layer 212 is removed while leaving catalyst layer 204 intact at the bottom of gate aperture 210 on substrate surface 203. Two methods may be used to accomplish this. The catalyst layer 204 at the bottom of gate aperture 210 is protected by first spinning a resist layer 224 over the cell structure 200 (Figure 2(d)). Next, isotropic etching with oxygen plasma or anisotropic oxygen RIE removes most of the resist layer 224 except for a portion on top of catalyst layer 204 at the bottom of gate aperture 210. Subsequently, acid dissolution removes catalyst layer 204 from all surfaces not protected by resist 224 (Figur 2(e)).

Alternatively, rather than depositing resist layer 224 followed by isotropic etching using oxygen plasma, catalyst layer 204 may be selectively removed from all surfaces except from the bottom of aperture 210 by glancing angle sputtering.

Nanofilaments 214 are grown (Figure 2(f)) and field emitter 200 is then dipped in hydrofluoric acid, rinsed in water, and freeze-dried (Figure 2(g)). The hydrofluoric acid rinse removes the upper (i.e., top) portion of stand-off layer 212 and undercuts insulator layer 206 in area 218. As with the first embodiment, the base of clump cathode 216 between nanofilaments 214 and the side-wall of aperture 210 may be optionally reinforced as described above. Alternatively, the upper portion of standoff layer 212 can be removed by dry etching, which least disturbs the nanofilaments.

3rd Embodiment

Referring now to Figures 3(a)-3(g), in a third embodiment, the starting substrate upon which the nanofilaments are grown is a post structure 330. Referring now specifically to Figure 3(a), post 330 is formed by patterning and reactive ion etching (RIE) a starting material of nanoporous silicon layer substrate 302 with catalyst layer 304. The patterning and RIE are standard microelectronic fabrication methods known in the art. Catalyst layer 304 is optionally oxidized in the same manner as in the earlier described embodiments.

Nanofilaments 314 are preferably carbon nanotubes that are grown on top of post 330 under the same conditions as in the previous embodiments, resulting in clump cathode 316 (Figure 3(b)). A conformal stand-off layer 312 composed of silicon nitride, silicon dioxide or tungsten, is deposited over the entire cell structure 300 structure (Figure 3(c)).

Referring now to Figure 3(d), planarization layer 332 is deposited over cell structure 300 along the top of stand-off layer 312. Planarization layer 332 is composed of a suitable insulator material such as silicon dioxide or spin-on glass of a different insulator material than that of stand-off layer 312. Standard planarization techniques such as chemical-mechanical-polishing (CMP) is performed on planarization layer 332 (Figure 3(d)).

Selective directional RIE is used to etch back planarization layer 332 to a desired height 334 below the top of stand-off layer 312 without etching the stand-off layer 312 (Figure 3(e)). The desired height 334 determines the placement of the control gate relative to clump cathode 316.

Referring now to Figure 3(f), gate metalization material is directionally evaporated on top of planarization layer 332 to form gate layer 308, and on the horizontal surface of stand-off layer 312 to form metalization cap 338. Care should be taken such that gate metalization material is not deposited on the vertical portions 313 of stand-off layer 312. If necessary, a short etch may be used to remove any material inadvertently deposited on the vertical portions 313 of stand-off layer 312.

Wet etch (such as by HF) or isotropic dry etch is carried out to remove the top portion 336 of stand-off layer 312. The wet etch or isotropic dry etch also removes metalization cap 338 as well as removing a portion of stand-off layer 312 below metalization cap 338, recessing stand-off layer 312 sufficiently below the top of clump cathode 316 (Figure 3(g)). If a wet etch is used, freeze-drying is used to remove the residual liquid.

4th Embodiment

Referring now generally to Figures 4(a)-4(i), a fourth embodiment is shown which represents a modification of the processing method of the third embodiment. In the fourth embodiment, a catalyst layer 404 is deposited on post 430 after gate layer 408 is formed.

Referring specifically now to Figure 4(a), post 430 is formed in a similar manner as post 330 with the exception that the starting structure is a post structure 430 on top of substrate 402 without a catalyst layer formed thereon. A silicon dioxide (SiO_2) stand-off layer 412 is thermally grown (in case

if the post and substrate are made of silicon) or deposited over cell structure 400 including the horizontal surfaces 403 of substrate 402 and horizontal and vertical surfaces of post 430 (Figure 4(b)). Subsequently, an insulator planarization layer 432, gate layer 408, and metalization cap 438 ar formed as in the third embodiment (Figure 4 (c)). A wet etch or isotropic dry etch removes the metalization cap 438, the top portion of the stand-off layer and undercuts planarization layer 432 in areas 418 (Figure 4(d).

Preferably, a thin conformal CVD silicon dioxide forms sacrificial layer 440 (Figure 4(e)) over all surfaces of the cell. Next, directional RIE is used to remove sacrificial layer 440 from the top of post 430 and the top of gate layer 408 while leaving the vertical sides of post 430 covered with the CVD silicon oxide sacrificial layer 440 (Figure 4(f)). It should be noted, however, that a sacrificial layer is not necessary to practice this embodiment of the invention.

Referring now to Figure 4(g), catalyst layer 404, such as nickel (Ni) which is relatively resistant to reaction with HF is directionally deposited by sputtering or evaporation on the top surfaces of cell structure 400 which include on top of post 430 and gate layer 408, as well as residually in gate aperture 410 along conformal sacrificial oxide layer 440. Optimally, under nanotube growth conditions, the material of gate layer 408 should alloy with or passivate the material of catalyst layer 404, thereby preventing nanofilament growth on gate layer 408. For example, the gate material may be chromium (Cr) which passivates Ni.

The cell structure 400 is briefly dipped in a dilute buffered HF solution to remove (i.e., lift off) any catalyst material which may lie on top of the sacrificial silicon dioxide layer 440 in aperture 410 (Figure 4(h)). The hydrofluoric acid removes both the unwanted catalyst present in aperture 410 as well as CVD silicon dioxide sacrificial layer 440 present in aperture 410 along the vertical wall surfaces of post 430 and along planarization layer 432 and gate layer 408. A significant amount of catalyst should remain on the top surface of the post 430.

Nanofilaments 414 are grown on top of post 430 under similar conditions as set forth in the previous embodiments, resulting in clump cathode 416 (see Fig. 4(i)).

One advantage of the fourth embodiment is that the nanofilament 414 placement can be above gate layer 408. Consequently, there is less probability that there will be a short between nanofilaments 114 and gate layer 408.

5th Embodiment

Figures 5(a)-5(d), depicted a fifth embodiment of the present invention. In this embodiment, nanofilament growth occurs on the top surface of a conventional tip-on post emitter (530) or conical tip emitter (531) known in the art. This embodiment differs from the fourth embodiment in that instead of using the blunt post structure of post 430, this embodiment uses ready-made conventional field emitter structures of sharpened tip-on-post structure or a conical tip structure upon which nanofilaments are grown. Otherwise, the processing steps of this embodiment are identical to that of the fourth embodiment.

A conformal silicon dioxide sacrificial layer is first deposited over field emitter cells 500, 501,and then selectively removed by directional RIE from the top surfaces of the tip-on-post 530, or conical tip 531, in a manner similar to that in the fourth embodiment. Optimally, the gate aperture 511 of the conical tip design is small as practicable and should be smaller than the diameter of the base of the conical cathode 531. It should be noted, however, that a sacrificial layer is not necessary to practice this embodiment of the invention.

Next, a catalyst is deposited, the sample treated with hydrofluoric acid, rinsed in water, and nanofilaments are grown along the top surface of tip-on-post 530, and conical tip 531 (Figures 5(c)

and 5 (d)), in similar manner as in the fourth embodiment. As a result, clump cathode 516 is formed of nanofilaments 514 protruding outward from the surface of the centers (i.e., upper portions) of tip-on post 530 (Figure 5 (c)) and conical tip 531 (Figure 5 (d)).

The lengths of the nanofilament 514 should be limited so that the nanofilaments ar relatively short and do not come into contact with other parts of the emitter (for example, the gate layer 508 or insulator 532). Preferably, the lengths of the nanofilaments should be a small fraction of the distance between the top of the original (tip-on- post or conical tip) to the edge of the gate aperture 510 and 511. Optimally, although not essential, tip-on post 530 and conical tip 531 should be of a material that does not passivate the catalyst material 504.

If the emitter tip material passivates the catalyst, the tip should be coated with a material that prevents diffusion of the catalyst material into the tip material under nanofilament growth conditions. As with the previous embodiments, it is preferable that the material of gate layer 508 does passivate the catalyst material so that no nanofilaments will grow on the gate layer 508.

If the gate material does not passivate the catalyst material, it is necessary to remove the catalyst material from the top surface and the edge of the gate. Sputtering at a glancing angle (small angle relative to the surface of the substrate) with an ion beam is one such way of removing the catalyst material. Care should be taken that the angle is such that no portion of the tip-on-post or conical tip is sputtered.

To remove catalyst material by lift-off process from any silicon dioxide surface (e.g., surfaces of remaining sacrificial silicon dioxide layer or the surface of the silicon dioxide insulator layer 532), the structure may be dipped in a buffered HF solution. However, the duration should be sufficiently short such that a significant amount of catalyst 504 still remains on the surfaces of the top portions of structures 530 and 531.

Optimally, nanofilaments 514 are grown on the portion of tip on-post 530 and conical tip 531 covered with catalyst layer 504 using CVD method under lean hydrocarbon conditions (i.e., low hydrocarbon-to-reducing gas ratio) to eliminate growth of non-nanofilament carbonaceous material on insulator layer 532. The growth time should be limited so that nanofilaments 514 should be relatively short.

If necessary, a short isotropic oxygen plasma, such as in a barrel etcher, can be used to remove any thin layer of carbonaceous material from insulator layer 532. If the insulator layer 532 is silicon dioxide, it can be optionally followed by a short dip in dilute buffered HF and subsequent water rinsed to ensure cleanliness of the surface of insulator 532.

Precautions should be taken to prevent any nanofilaments 504 from lying down on the tip surface due to adhesion (stiction) after exposure to an aqueous environment of HF and water rinse. As with the previous embodiments, it is optimal to use a freeze-drying or a critical-point drying technique.

An exemplary preferred implementation of the processing method of the fifth embodiment will now be considered. It will be understood that this example is provided to enhance understanding of the present invention and not to limit the scope or adaptability thereof.

The starting structures were an array of the silicon tip-on-post gated field emitter cells fabricated according to a process developed at the Microelectronic Center of North Carolina by a number of standard silicon microprocessing steps (outlined in Fig.3 in D. Temple, et. al., J. Vac. Sci. Technol. B 13, 150 (1995) and in Fig. 2 in L.N. Yadon, et. al., J. Vac. Sci. Technol. B 13, 580 (1995)). The silicon tip-on-post emitter cell structure is schematically shown in Fig. 5(a) of the present disclosure.

The silicon post height was about 4 microns, the post diameter was about 1 micron, and the post was topped with a very small and sharp conical silicon tip. The gate aperture diameter was 2.8 microns and the gate material was made of pure chromium, which apparently could survive the relatively high temperatures and conditions used for carbon nanotube (cNT) growth in the current example. Moreover, chromium, under the cNT growth conditions used in this example, has been observed to passivate Fe and Ni catalysts (e.g. no cNT growth on Fe and Ni –coated chromium surfaces). It was optional to omit the initial deposition of a conformal sacrificial silicon dioxide layer. In this example, the initial conformal silicon dioxide sacrificial layer had been omitted.

Next, a very thin layer of nickel catalyst was sputter-deposited on the substrate using an ion beam and a nickel foil as sputtering target. The nickel coated the surfaces of the chromium gate, the top surface of the tip-on-post (including the small silicon tip), and likely residually other surfaces in the emitter cell cavity. The sample was then briefly dipped in a dilute buffered HF solution and thoroughly rinsed (by weak ultrasonication) in distilled water. The HF removed (by lift-off) much of the residual nickel that happened to be on any silicon dioxide surfaces in the emitter cell cavity. After drying by blowing with nitrogen and mild heating on a hot plate, the sample was placed on the flat top of a molybdenum cartridge heater in a hot filament chemical vapor deposition (CVD) flow reactor, in which the hot filament consisted of a tungsten ribbon suspended parallel to and about a centimeter above the sample. The cartridge heater and the tungsten filament were heated separately. The temperature was measured by a thermocouple in contact with the top surface of the cartridge heater. The gas flow was perpendicular to the surface of the sample.

Growth of the carbon nanotube emitters began by first heating the sample in flowing argon at a pressure of about 20 torr until a temperature of about 700°C was reached, at which ammonia gas at a flow rate of 80 sccm replaced the argon and flowed onto the sample. The hot filament was immediately turned on and maintained at a filament temperature of about 1900°C as monitored by an optical pyrometer. Five minutes after turning on the hot filament, ethylene gas at a flow speed of 20 sccm was admitted into the flow reactor. The final temperature and pressure were maintained at 683°C and 23.3 torr, respectively. The hot filament, the ethylene gas, and ammonia gas were shut off 4.5 minutes after the admission of the ethylene gas. Argon at about 25 torr was then flowed as the sample was cooled down slowly.

Scanning electron microscope examination showed carbon nanotubes on the top surface of the tip-on post cathode structure and no carbon nanotubes on the chromium gate.

The sample was subjected to field emission test in an ultra-high vacuum chamber equipped with electrically conductive cathode, gate, and anode probes to provide electrical contact to the individual pixels (arrays) of the field emitter and to measure the current of the field-emitted electrons. For a pixel consisting of 33,000 emitter cells, the collected emission current (anode current) was measured as a function of the voltage applied to the gate electrode (with the cathode at ground). The results are shown in Figure 5(e).

An important result is the low turn on voltage (e.g. ~17 volts) compared to about 80 volts obtained for an array of silicon tip-on post FEA (without the nanotubes). The result for the latter sample is consistent with the 80-90 volts required by the silicon tip-on post structures in references by D. Temple, et. al., and L.N. Yadon, et. al. (above mentioned). This low turn-on voltage for the present nanotube-decorated example can be attributed to the carbon nanotubes acting as field emitters.

There can be a wide latitude on the growth parameters, such as different catalysts (e.g. Fe, Co), temperatures (500-1000°C), hydrocarbons (e.g. methane, acetylene), reducing agents (hydrogen), flow rates, pressures, and even a variety of growth techniques including thermal,

microwave, and RF CVD methods as well as arc and laser-assisted catalytic growth methods. In a CVD method, a low hydrocarbon-to-reducing agent ratio is necessary to minimize amorphous carbon deposition on catalyst-free surfaces, to avoid electrically shorting out the emitter cell (between cathode and gate).

6th Embodiment

In a sixth embodiment, the control gate is formed as offset gate aperture 609 in which the gate aperture is offset by distance 650 from the edge of the aperture 611 in insulator layer 606 (see Figure 6(a). The offset of a gate aperture from that of the insulator layer has previously been described in Patent Application Serial No. 09/478,899 filed on January 7, 2000.

The sixth embodiment is based on the second embodiment. All processing steps are the same as those in the second embodiment except that the starting cell structure has an off-set gate aperture. A similar offset of gate aperture 609 from the insulator aperture 611 formed therebelow may also be incorporated into the other embodiments. Likewise, other embodiments of gate offset in Patent Application Serial No. 09/478,899 are also incorporated into the present embodiment and other embodiments of the present invention as applicable. One possible advantage of having an offset gate layer is to reduce the gate current by precluding a direct-line-of sight from the nanofilament emitter to the gate.

An exemplary preferred implementation of the processing method of the sixth embodiment will now be considered. It should be understood that this example is provided to enhance understanding of the present invention and not to limit the scope or adaptability thereof.

The starting structure was similar to that shown in Fig 2(a), except that the gate was offset (having a larger diameter than that of the hole in the insulator layer). The methods for fabricating starting structures with offset gates were also given in a commonly-owned patent application (Patent Application Serial No. 09/478,899). The gate material consisted of a 60 nm thick chromium layer on top of a 150 nm thick p-type silicon layer. The hole in the insulator layer had a diameter of 1.2 microns and the gate diameter was 2.25 microns (e.g. the offset was about 0.5 micron). A stand-off CVD silicon dioxide layer (nominally 0.42 micron thick on top flat surface) was then deposited over the structure, followed by oxide etch back by RIE of 0.45 micron of silicon dioxide. SEM analysis showed a 0.32 micron thick stand-off layer on the vertical sidewall of the hole, leaving an open, inner hole of about 570 nm diameter.

A thin layer of Fe was then deposited over the sample using an ion beam and a Fe foil as sputtering target. Next, a 0.25 micron thick Shipley 1400 photoresist was spin-coated over the sample, followed by baking at 90°C for 30 minutes. Oxygen plasma using a barrel etcher was used to remove the resist from the top horizontal surface and from the upper portion of the hole. The exposed Fe was removed by dipping the sample in an acid solution. After rinsing in water and drying, the sample was ultrasonicated in acetone, followed by ethanol to remove the resist from the bottom portion of the hole, thereby exposing the Fe catalyst on the bottom portion of the hole.

The growth of the carbon nanotube emitters was carried out under similar conditions as described above in reference to the exemplary implementation of the fifth embodiment, except a DC voltage bias was placed on the hot filament with respect to the top surface of the cartridge heater and that a growth duration of only 40 seconds was used. The purpose of the voltage bias was to promote more oriented growth of the carbon nanotubes.

Field emission test was carried out on a small pixel of an array of 20 emitter cells. The anode current and the gate current were measured simultaneously as a function of the voltage applied to the gate electrode. The results are shown in Figure 6(b). A turn-on voltage below 35 volt was observed.

Figure 6(b) also shows that the gate current is a very small fraction of the anode current, a result expected from an offset gate design. An offset gate can also be expected to require a higher turn-on voltage than one without an offset.

Alternative photoresist etching could be done by oxygen reactive ion etching (which is anisotropic) instead of by the oxygen barrel etcher (which is isotropic), thereby gaining better control over the portion of resist to be removed.

7th Embodiment

In a seventh embodiment, the starting substrate is the same post structure used in Embodiment 3, with a preformed catalyst layer on top (such as shown in Figure 3(a)), fabricated by standard microelectronic processing known in the art. Optionally the catalyst layer has a protection layer (such as silicon nitride) above it to help preserve it during the ensuing processing. The method of this embodiment is similar to that of the 3rd Embodiment except that the nanofilaments are grown on top of the post structure after the gate structure has been formed.

After a standoff layer is deposited over the starting substrate with the above-mentioned post structure and catalyst layer on top, the same planarization, gate structure formation and insulator undercutting processes are carried out as in the 3rd Embodiment (and 4th Embodiment), resulting in the structure shown in Figure 7(a) (which is similar to Figure 4(d) except the post structure has a catalyst layer on its top surface). At this point, any optional protection layer on top of the catalyst layer is removed.

Nanofilaments 714 are grown on top of post 730 under similar conditions as set forth in the previous embodiments, resulting in a group of nanofilaments as a clump cathode 716 (see Fig. 7(b)).

8th Embodiment

The method of the 8th Embodiment is similar to the 2nd Embodiment except that the masking layer is not used. However, it is necessary that the gate layer be composed of a material that passivates the catalyst. The same processing steps for the standoff layer formation used in the 2nd Embodiment (Fig. 2(a)-(c)) are used in the 8th embodiment which leads to the structure found in Fig. 8(a). Optionally, at this point, a sacrificial silicon dioxide insulator layer (not shown in Fig. 8(a)) can be deposited and directionally etched back to clear the substrate at the bottom surface 803 of the cell aperture. It is critical here, however, that surface 803 of the substrate does not passivate the catalyst. A catalyst layer 804 is directionally deposited over the resulting cell structure. (See Fig. 8(b)). Some catalyst is likely to be unavoidably deposited over the sidewalls of the aperture.

Next, a wet etch liftoff is performed to remove the catalyst from the sidewalls as well as the top surface of the standoff layer 812 (such as using hydrofluoric acid if the standoff layer or the optional sacrificial layer is composed of silicon dioxide), resulting in a structure with a significant amount of catalyst layer 804 left intact on the bottom surface 803 of the aperture as shown in Fig. 8(c). The material of the substrate surface 803 has different wet etch properties than the standoff layer or the sacrificial layer so that the same wet etch does not liftoff the catalyst from surface 803.

Growing the nanofilaments 814 and recessing the standoff layer and insulator layer as in the previous embodiments results in the emitter structure with a group of nanofilaments as a clump cathode 816 as shown in Fig. 8(d).

Although the invention has been described above in relation to preferred embodiments thereof, it should be understood by those skilled in the art that variations and modifications can be effected in these preferred embodiments without departing from the scope and spirit of the invention.

CLAIMS

What is claimed is:

1. A method of manufacturing a field emitter cell, comprising the steps of:

providing a conductive substrate layer;

forming a catalyst layer on said conductive substrate layer;

forming an insulating layer either on an upper surface of said catalyst layer or directly on said substrate layer;

forming a conductive gate layer on an upper surface of said insulating layer;

making at least one perforation through said gate layer that extends downward into said insulating layer thereby forming a gate aperture in said gate layer, with said perforation comprising sidewalls and being in electrical contact with either said catalyst layer or substrate layer;

forming a standoff layer on said gate layer, said sidewalls, and said catalyst layer or substrate layer;

removing the portion of said standoff layer on said gate layer, catalyst or substrate layer while retaining said standoff layer on said sidewalls; and

growing an electrically conductive group of nanofilaments on said catalyst layer conductively associated with said substrate layer, said group of nanofilaments being electrically isolated from the said gate layer.

2. The method of claim 1, wherein a top portion of said retained standoff layer is optionally removed to provide a vacuum gap between said group of nanofilaments and both said insulator layer and said gate aperture.

3. The method of claim 1, wherein the growing of said group of nanofilaments results in a self-alignment between said gate aperture and said group of nanofilaments;

4. The method of claim 1, wherein said catalyst layer is deposited on said substrate layer prior to formation of said insulator layer.

5. The method of claim 2, wherein the step of removing a top portion of said retained standoff layer is conducted by the process of dry etching.

6. The method of claim 2, wherein said step of removing a top portion of said retained standoff layer comprises the sub-steps of:

rinsing with a selective wet etch solution and water; and

freeze-drying to remove residual water.

7. The method of 1, wherein the step of providing a conductive substrate layer involves the formation of a nanoporous silicon substrate layer.

8. The method of claim 1, wherein said step of forming a catalyst layer on said conductive substrate layer comprises a method selected from the group consisting of sputtering deposition, physical evaporation, dipping in a colloid suspension of catalyst nanoparticles, and coating with a salt solution of the catalyst metal followed by reduction to metal.

9. The method of claim 1, wherein said step of forming said catalyst layer involves oxidation of the catalyst.

10. The method of claim 1, wherein said gate layer is composed of materials selected from the group consisting of a conductive substance, p-type semi-conductor, n-type semi-conductor, and multiple layered combinations thereof.

11. The method of claim 1, wherein formation of said catalyst layer on said substrate layer occurs after the step of removing a portion of said standoff layer on said gate layer and said substrate layer while retaining the standoff layer on the sidewalls, and comprises the steps of:

depositing said catalyst layer over said gate layer, said standoff layer, and said substrate layer on the bottom of said perforation;

depositing a masking layer over all exposed surfaces so that said masking layer is thicker over said catalyst layer on the bottom of said perforation than on said gate layer or upper portions of said retained standoff layer;

removing said masking layer from said gate layer and upper portions of said retained standoff layer, while preserving enough masking layer thickness to cover said catalyst layer on the bottom of the perforation;

removing the now exposed said catalyst layer from said gate layer and the upper portions of said retained standoff layer, while leaving said catalyst layer under the remaining said masking layer intact; and

prior to growing said nanofilaments, removing said remaining masking layer from said bottom of the perforation and thereby exposing remaining said catalyst layer.

12. The method of claim 1, wherein said step of making a perforation through the gate layer comprises forming an offset gate aperture, said offset gate aperture having dimensions larger than those of said perforation through the insulator layer.

13. The method of claim 1, wherein said step of forming a gate aperture involves the formation of said gate aperture having dimensions either larger, smaller, or equivalent to the dimensions of said perforation through the insulator layer, said perforation having a second standoff layer shielding an edge of the gate aperture.

14. The method of claim 1, wherein said conductive gate is composed of a either a single or multiple layer material that is capable of passivating said catalyst layer.

15. The method of claim 1, wherein said step of forming the conductive gate layer comprises forming the gate layer from a metal selected from the group consisting of chromium, tungsten, platinum, tantalum, molybdenum, and combinations thereof.

16. The method of claim 1, wherein said gate layer is composed of a material that passivates said catalyst, and said step of forming said catalyst layer on said substrate layer occurs after the step of removing a portion of said standoff layer on said gate layer and said substrate layer while retaining the standoff layer on the sidewalls, and comprises the steps of:

depositing said catalyst layer over said gate layer, said standoff layer, and said substrate layer

on the bottom of said perforation; and

prior to growing said nanofilaments, removing said catalyst layer by a lift-off process from said sidewall and said top portions of said retained standoff layer, while leaving significant catalyst layer on the bottom surface of the perforation intact.

17. The method of claim 16, wherein a sacrificial CVD silicon dioxide layer is deposited and then directionally etched back to expose the substrate surface at the bottom of the aperture before said catalyst layer is deposited.

18. A method of manufacturing a field emitter cell, comprising the steps of: providing a conductive substrate layer having at least one raised structure thereon, said raised structure being conductively associated with said substrate layer and having an upper surface and sidewalls;

forming a catalyst layer conductively associated with said raised structure;

providing an insulating layer; and

forming a conductive gate layer over said insulating layer, said conductive gate layer having a gate aperture horizontally surrounding said raised structure and extending downward into said insulating layer; and

growing a conductive group of nanofilaments on said catalyst layer, said group of nanofilaments being electrically isolated from said gate layer.

19. The method of claim 18, wherein said raised structure is a post structure with sidewalls and an upper surface with a preformed catalyst layer, whereon the formation of a group of nanofilaments occurs on said upper surface before said gate aperture is formed, and said formation of gate aperture and other critical portions of said field emitter cell comprises steps of:

forming a standoff layer over said upper surface, said sidewalls, and said nanofilaments;

depositing said insulating layer over said standoff layer, said insulating layer having a height greater at all points than top portion of said standoff layer, upper surface of said post structure, and said nanofilaments;

planarizing the insulating layer to provide a planarized structure in which said planarized insulating layer is over said top portion of the standoff layer;

selectively removing a top portion of said planarized insulating layer so that an upper surface of said insulating layer is below the top upper surface of said post structure, thereby exposing said top portion of the standoff layer and at least a fraction of sidewalls of said standoff layer;

forming said conductive gate layer over said insulating layer and said exposed top portion of the standoff layer; and

selectively etching said standoff layer, thereby removing the portion of said gate layer located on said top portion of the standoff layer and additional portions thereof, thereby providing a vacuum gap between said insulating layer and an upper portion of said group of nanofilaments, thereby establishing electrical isolation between said gate layer and said group of nanofilaments.

20. The method of claim 19, wherein the step of selective etching of said standoff layer comprises dry etching.

21. The method of claim 19, wherein the step of selective etching of said standoff layer

comprising the steps of:

rinsing with a selective wet etching solution and water; and

freeze-drying to remove residual water.

22. The method of claim 18, wherein said raised structure is a post structure with sidewalls and an upper surface, and wherein formation of said catalyst layer and said formation of a group of nanofilaments comprises steps of:

forming a standoff layer over said upper surface and said sidewalls;

depositing said insulating layer over said standoff layer, said insulating layer having a height greater at all points than top portion of said standoff layer and upper surface of said post structure;

planarizing the insulating layer to provide a planarized structure in which said planarized insulating layer is over said top portion of the standoff layer;

selectively removing a top portion of said planarized insulating layer so that an upper surface of said insulating layer is below the top upper surface of said post structure, thereby exposing said top portion of the standoff layer and at least a fraction of sidewalls of said standoff layer;

forming said conductive gate layer over said insulating layer and said exposed top portion of the standoff layer, said gate layer comprising a material that passivates said catalyst layer;

selectively etching said standoff layer, thereby removing the portion of said gate layer located on said top portion of the standoff layer and additional portions thereof, thereby providing a vacuum gap between said insulating layer and an upper portion of said sidewalls of the post structure;

selectively etching to form an undercut in said insulator layer underneath said gate aperture;

depositing a conformal sacrificial layer on all exposed cell surfaces;

removing by directional etching portions of said sacrificial layer covering said upper surface of the post structure;

directionally depositing said catalyst layer on said upper surface of the post structure; and

prior to growing said nanofilaments, removing by a lift-off process said catalyst layer that is located over remaining portions of said sacrificial layer and said top surfaces of said standoff layer, while retaining said catalyst layer on said upper surface of said post structure and of said gate layer.

23. The method of claim 22, wherein the step of selective etching of said standoff layer comprises dry etching.

24. The method of claim 22, wherein the step of selective etching of said standoff layer comprising the steps of:

rinsing with a selective wet etching solution and water; and

freeze-drying to remove residual water.

25. The method of claim 22, wherein the step of depositing the sacrificial layer comprises deposition of silicon dioxide by CVD.

26. The method of claim 22, wherein the step of removing said catalyst layer and sacrificial layer comprises use of wet etching.

27. The method of claim 18, wherein said raised structure is a post structure with sidewalls and an

upper surface with a preformed catalyst layer, and wherein said method of manufacturing a field emitter cell further comprises the steps of:

forming a standoff layer over said preformed catalyst layer and said sidewalls;

depositing said insulating layer over said standoff layer, said insulating layer having a height greater at all points than top portion of said standoff layer and upper surface of said post structure;

planarizing the insulating layer to provide a planarized structure in which said planarized insulating layer is over said top portion of the standoff layer;

selectively removing a top portion of said planarized insulating layer so that an upper surface of said insulating layer is below the top upper surface of said post structure, thereby exposing said top portion of the standoff layer and at least a fraction of sidewalls of said standoff layer;

forming said conductive gate layer over said insulating layer and said exposed top portion of the standoff layer;

selectively etching said standoff layer, thereby removing the portion of said gate layer located on said top portion of the standoff layer and additional portions thereof, thereby providing a vacuum gap between said insulating layer and an upper portion of said sidewalls of the post structure; and

prior to growing said nanofilaments, selectively etching to form an undercut in said insulator layer underneath said gate aperture.

28. The method of claim 27, wherein said catalyst layer has a protective layer, said protective layer having different etching properties from the standoff layer, and is removed before the nanofilaments are grown.

29. The method of claim 18, wherein said raised structure is either a tip-on-post cathode or a conical tip cathode and the formation of said catalyst layer and said nanofilaments comprises the steps of:

providing a standard gated tip-on-post field emitter cell or a standard gated conical tip field emitter cell whose gate comprises a material that passivates said catalyst layer, said standard field emitter cells having a well-formed undercut cavity in the insulator layer and symmetrically oriented with the gate opening;

depositing a conformal sacrificial layer on all exposed surfaces of said standard field emitter cells;

removing said sacrificial layer from top portions of said tip-on-post cathode or conical tip cathode;

removing said catalyst layer on top of remaining said sacrificial layer, while retaining said catalyst layer on said top portions of the tip-on-post cathode or conical tip cathode and the gate layer; and

growing an electrically conductive group of nanofilaments on those portions of said catalyst layer still remaining on said tip-on-post cathode or conical tip cathode, said group of nanofilaments being electrically isolated from said gate layer.

30. The method of claim 18, wherein said group of nanofilaments is self-aligned with the gate aperture.

31. The method of claim 18, wherein the step of forming a catalyst layer comprises a method

selected from the group consisting of sputtering deposition, physical evaporation, dipping in a colloid suspension of catalyst nanoparticles, and coating with a salt solution of the catalyst metal followed by reduction to metal.

32. The method of claim 18, wherein the step of forming a catalyst layer involves oxidation of the catalyst layer.

33. The method of claim 18, wherein said gate layer is composed of materials selected from the group consisting of a conductive substance, p-type semi-conductor, n-type semi-conductor, and multiple layered combinations thereof.

34. The method of claim 18, wherein said conductive gate is composed of a either a single or multiple layer material that is capable of passivating said catalyst layer.

35. The method of claim 18, wherein said gate layer is formed from a metal selected from the group consisting of chromium, tungsten, platinum, tantalum, molybdenum, and combinations thereof.

36. The method of claim 1, wherein said step of growing nanofilaments is conducted by a catalytic reaction between a reactant gas or gases and said catalyst layer.

37. The method of claim 36, wherein said step of growing nanofilaments is conducted under an applied DC electric field.

38. The method of claim 36, wherein said catalytic reaction is accomplished using a CVD method.

39. The method of claim 18, wherein said step of growing nanofilaments is conducted by a catalytic reaction between a reactant gas or gases and said catalyst layer.

40. The method of claim 39, wherein said step of growing nanofilaments is conducted under an applied DC electric field.

41. The method of claim 39, wherein said catalytic reaction is accomplished using a CVD method.

42. The method of claim 1, wherein said nanofilaments are composed of material selected from the group consisting of carbon nanotubes, nanowires of doped or undoped Si, Ge, SiC, GaAs, GaP, InAs, InP, ZnS, ZnSe, CdS, CdSe, MoS_2, WS_2, and combinations thereof.

43. The method of claim 18, wherein said nanofilaments are composed of material selected from the group consisting of carbon nanotubes, nanowires of doped or undoped Si, Ge, SiC, GaAs, GaP, InAs, InP, ZnS, ZnSe, CdS, CdSe, MoS_2, WS_2, and combinations thereof.

44. The method of claim 1, wherein said perforation has a horizontal cross-sectional geometric shape selected from the group consisting of circular, linear, square, rectangular, and polygonal.

45. The method of claim 18, wherein said raised structure has a horizontal cross-sectional

geometric shape selected from the group consisting of circular, linear, square, rectangular, and polygonal.

46. The method of claim 2, wherein the removal of the top portion of said retained standoff layer, if insulating, is optional.

47. The method of claim 18, wherein the step of providing said raised structure includes the formation of a nanoporous silicon substrate layer on the upper surface of said raised structure.

48. The method of claim 1, wherein growing said group of nanofilaments further includes their doping, adsorbing another material, alloying, or carbide, halide, nitride, or oxide compound formation, thereby producing sufficient resistance to limit the emission current by causing an IR drop in the potential between the gate and the group of nanofilaments.

49. The method of claim 18, wherein growing said group of nanofilaments further includes their doping, adsorbing another material, alloying, or carbide, halide, nitride, or oxide compound formation, thereby producing sufficient resistance to limit the emission current by causing an IR drop in the potential between the gate and the group of nanofilaments.

50. A method of manufacturing a field emitter cell, comprising the steps of:

providing an conductive substrate layer;

forming a catalyst layer on said conductive substrate layer;

forming an insulating layer either on an upper surface of said catalyst layer or directly on said substrate layer;

forming a conductive gate layer on an upper surface of said insulating layer;

making at least one perforation through said gate layer that extends downward into said insulating layer thereby forming a gate aperture in said gate layer, with said perforation comprising sidewalls and being in electrical contact with either said catalyst layer or substrate layer; and

growing an electrically conductive group of nanofilaments on said catalyst layer conductively associated with said substrate layer, said nanofilaments being electrically isolated from said gate layer.

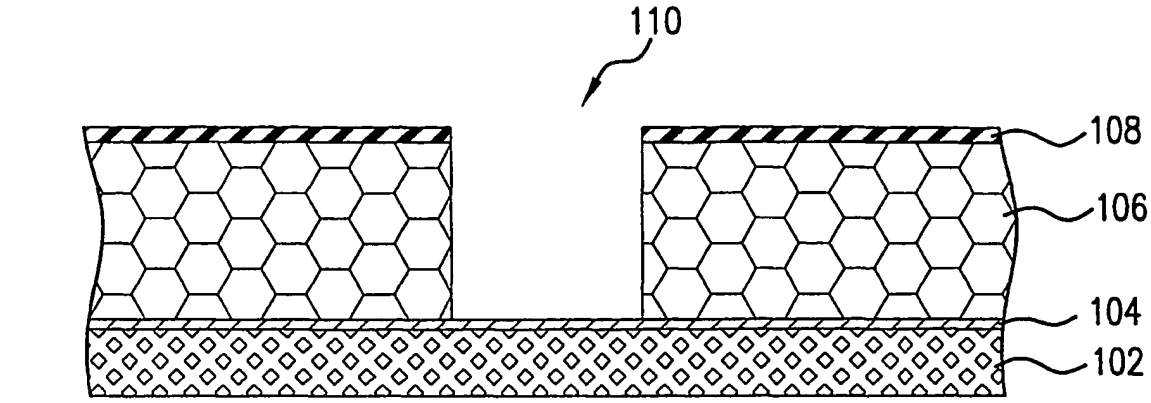


FIG. 1a

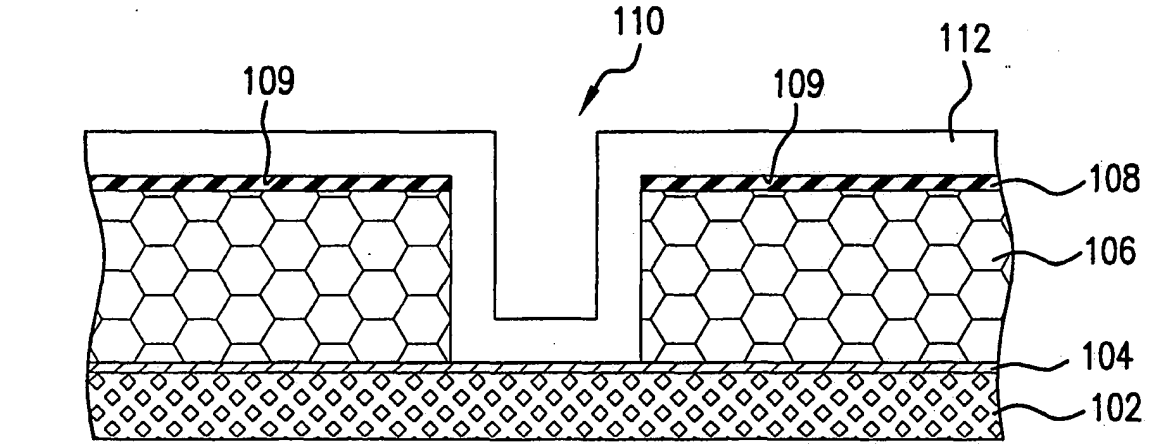


FIG. 1b

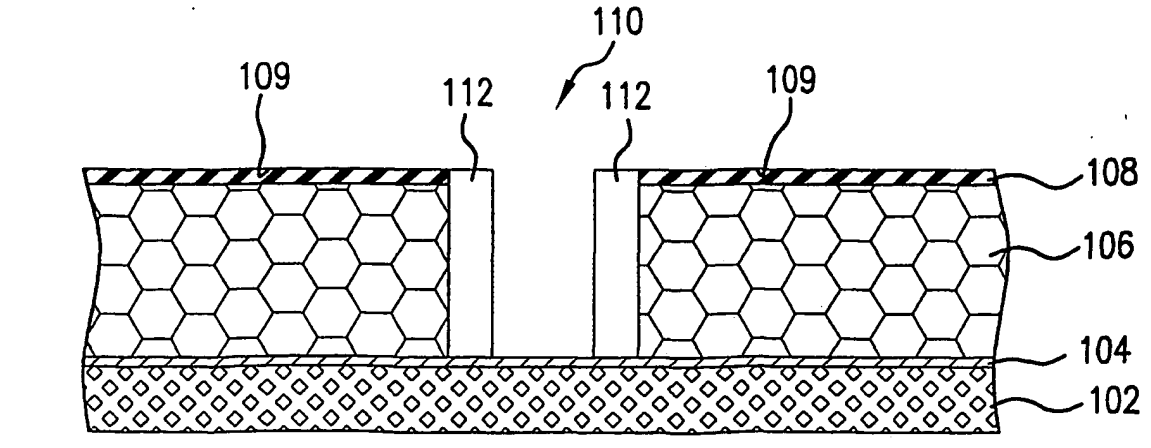
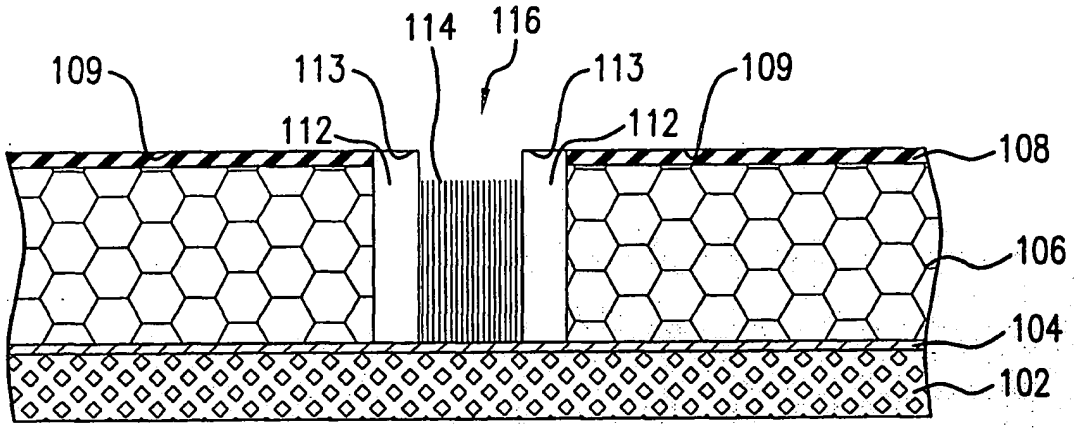


FIG. 1c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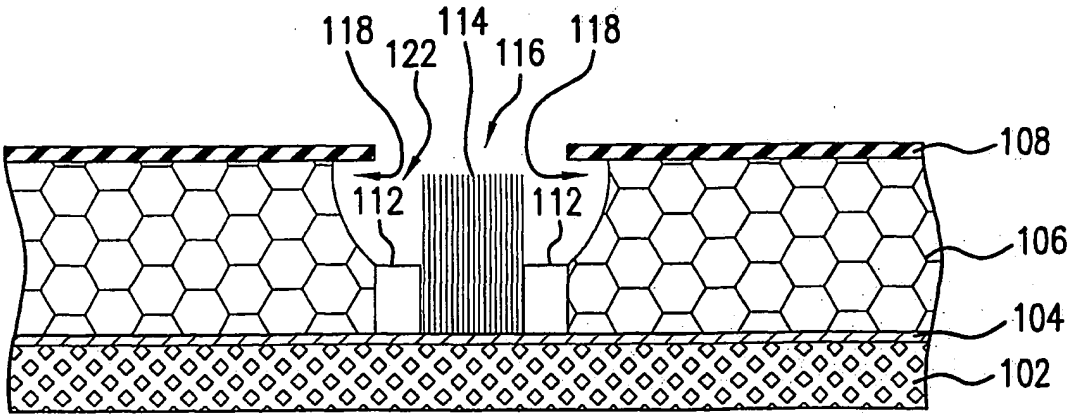
102
100

FIG. 1d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102
100

FIG. 1e

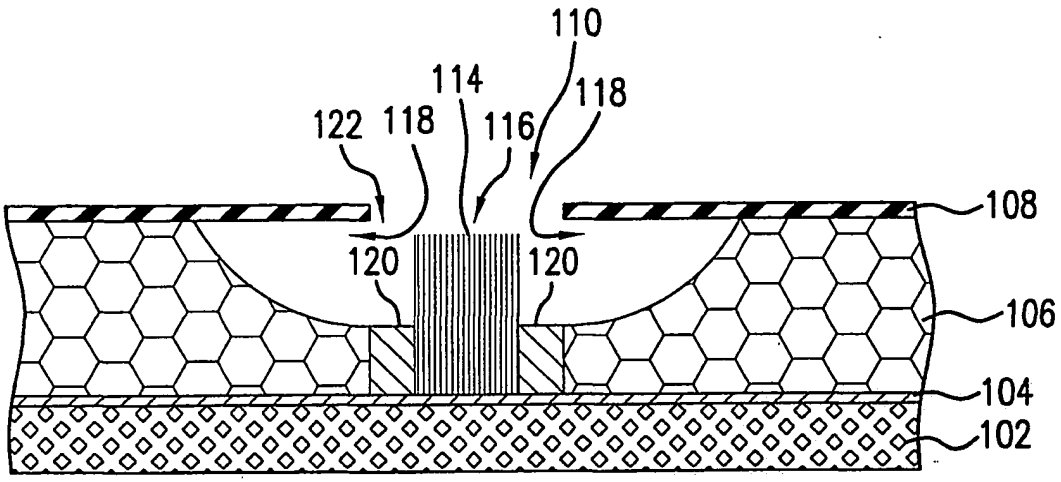

FIG. 1f

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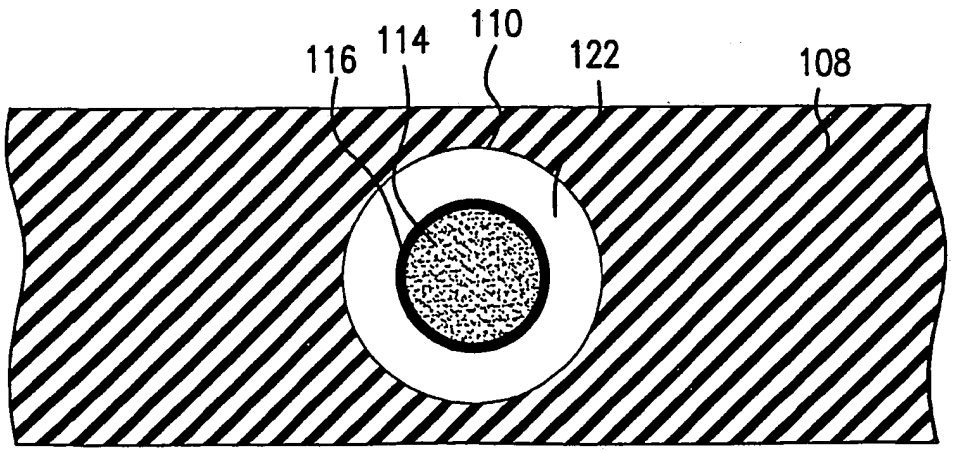

FIG. 1g

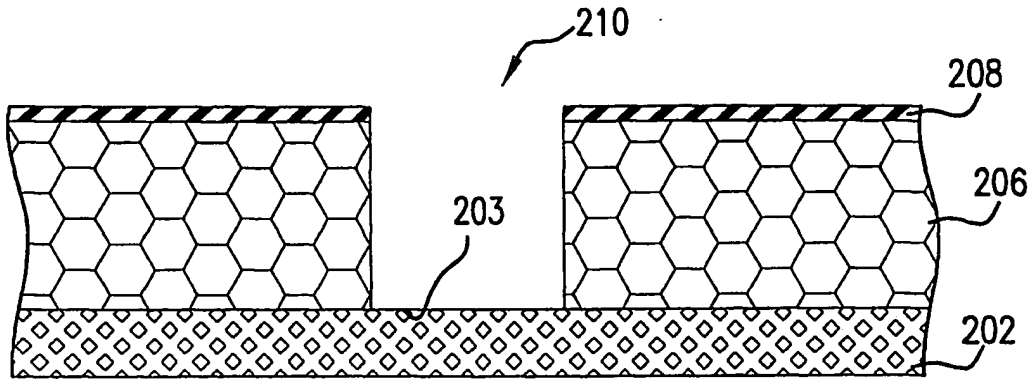

FIG. 2a

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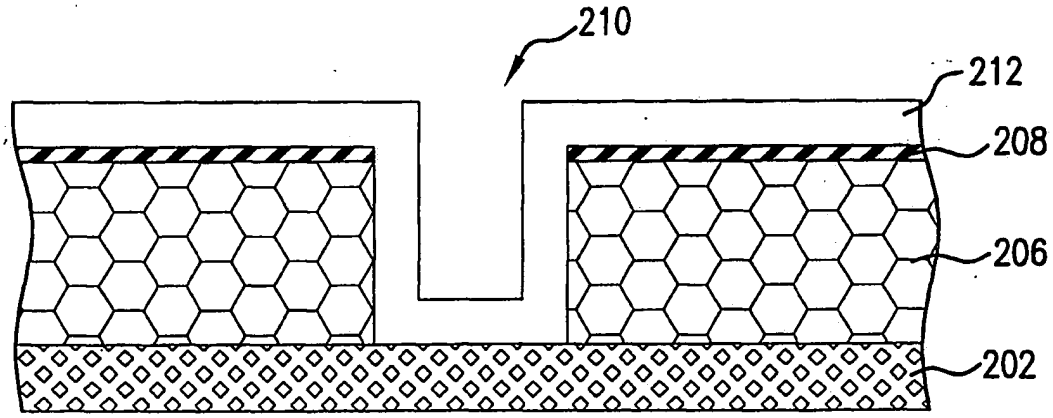


FIG. 2b

200

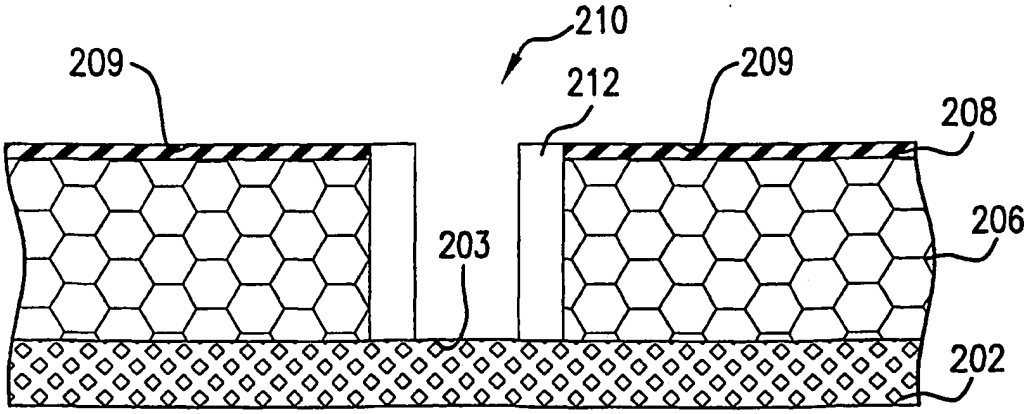


FIG. 2c

200

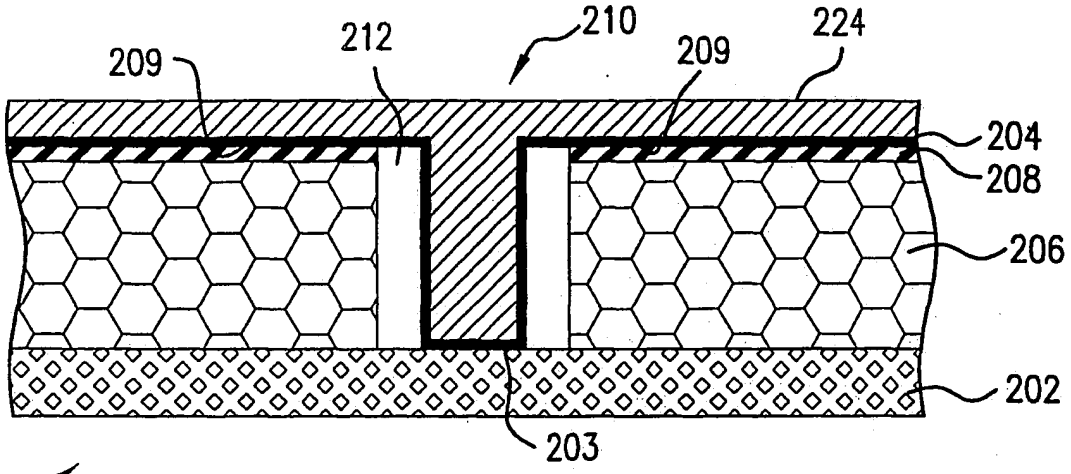


FIG. 2d

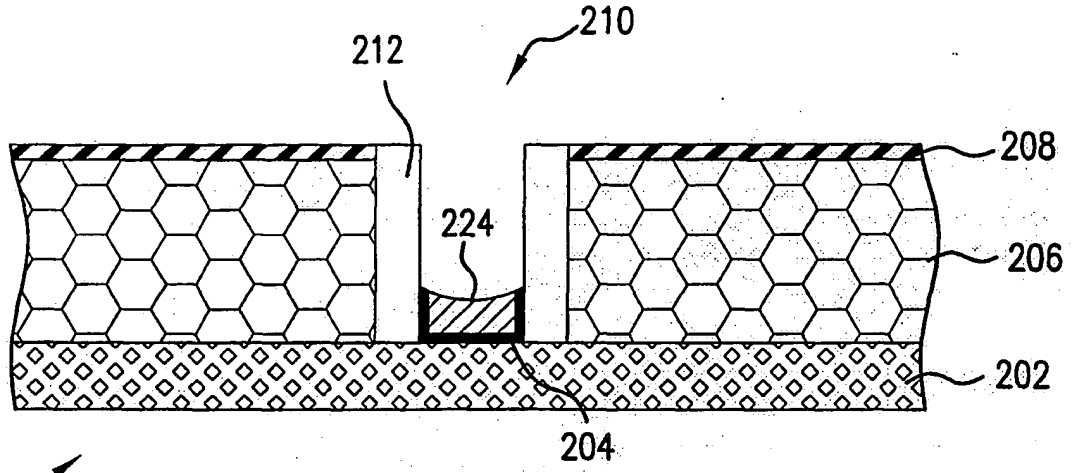


FIG. 2e

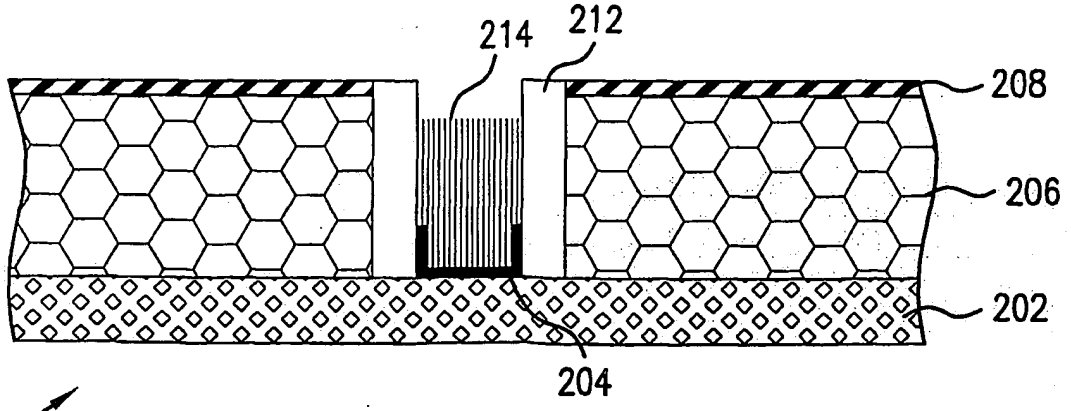


FIG. 2f

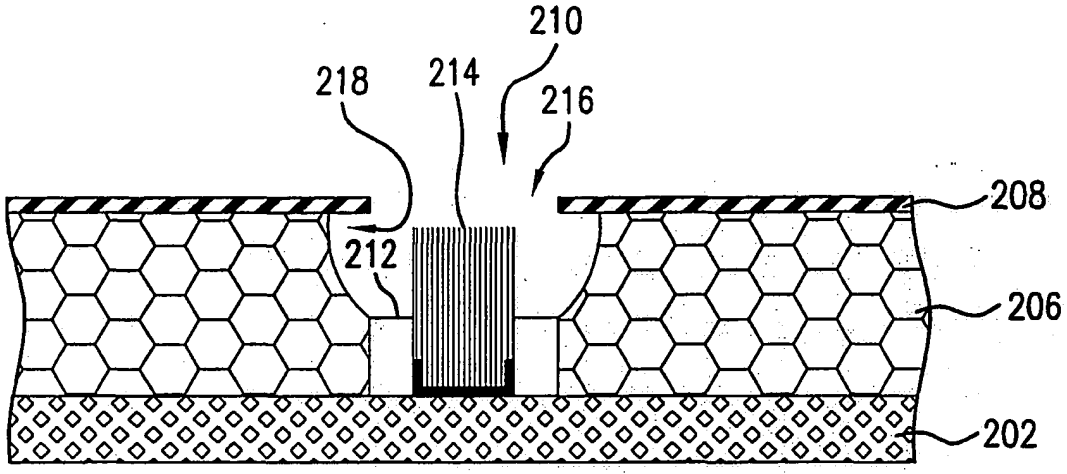


FIG. 2g

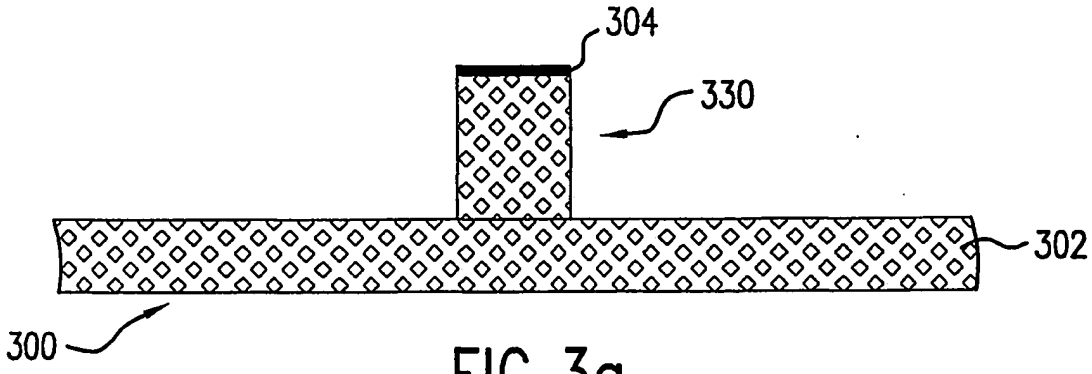


FIG. 3a

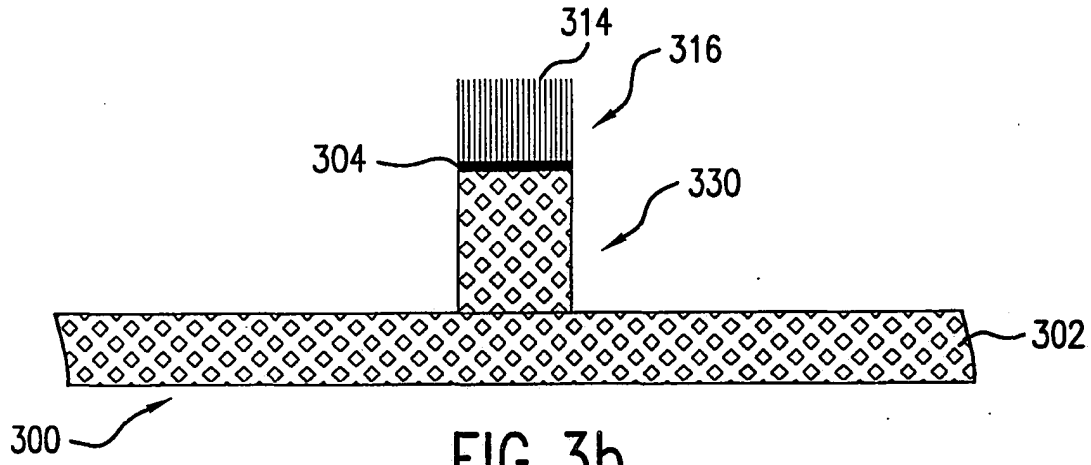


FIG. 3b

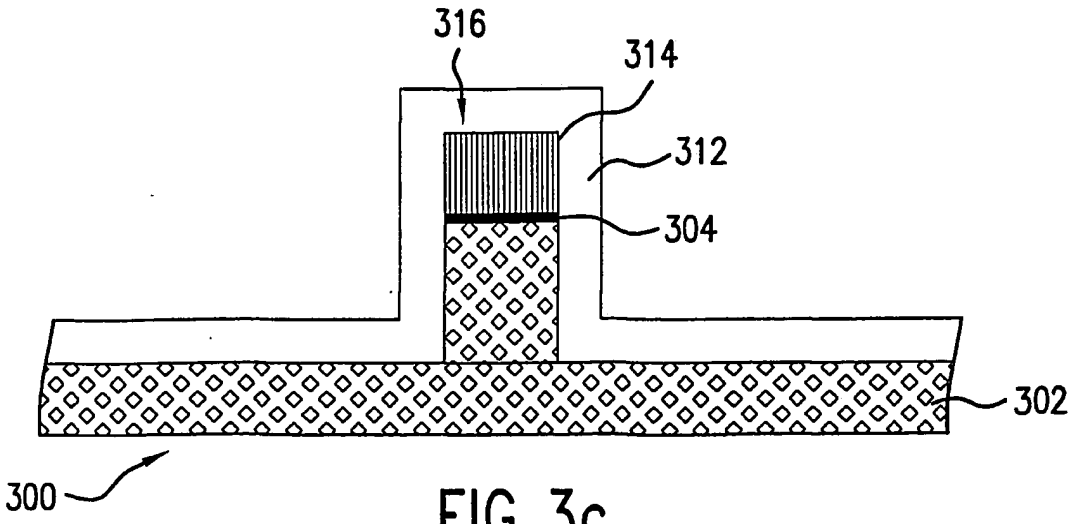


FIG. 3c

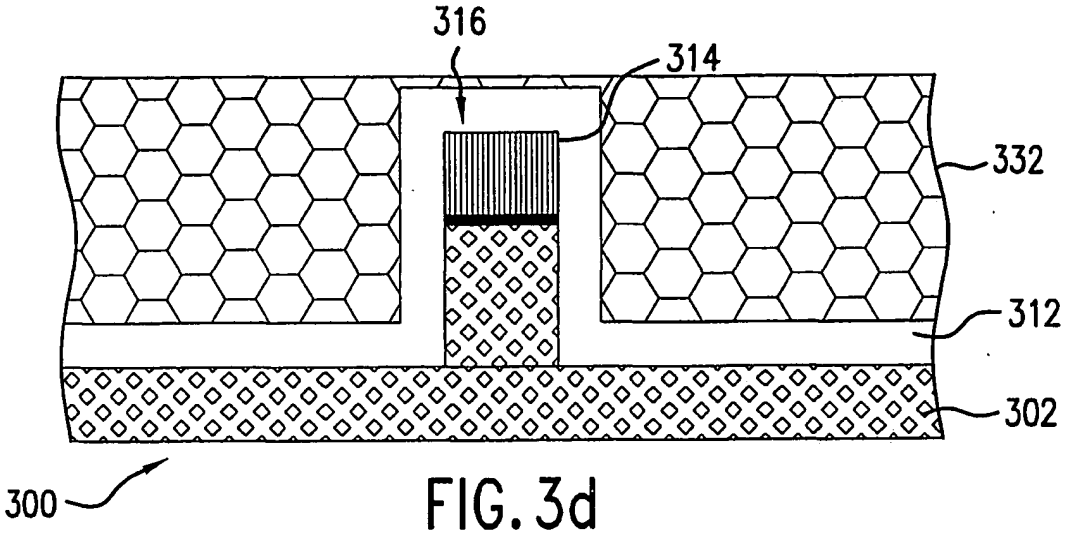


FIG. 3d

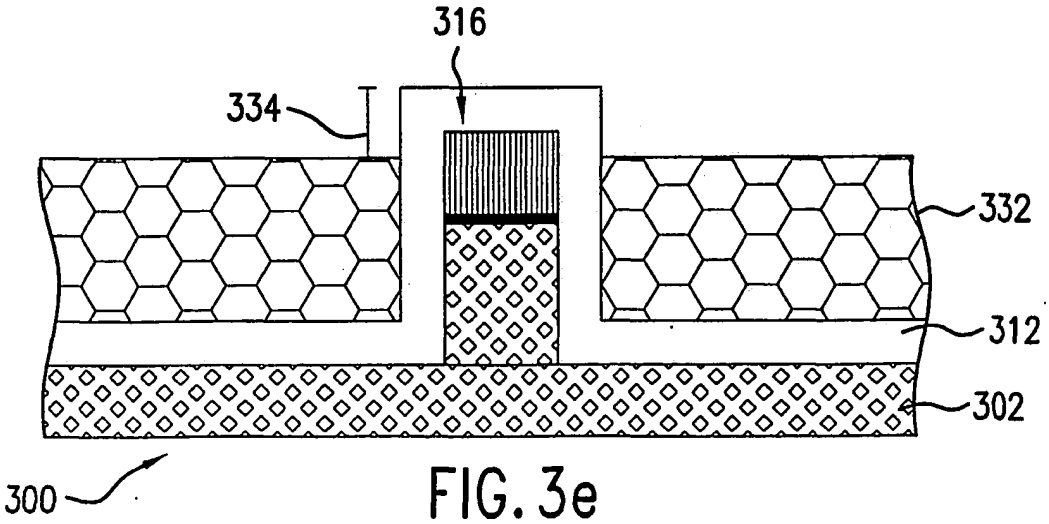
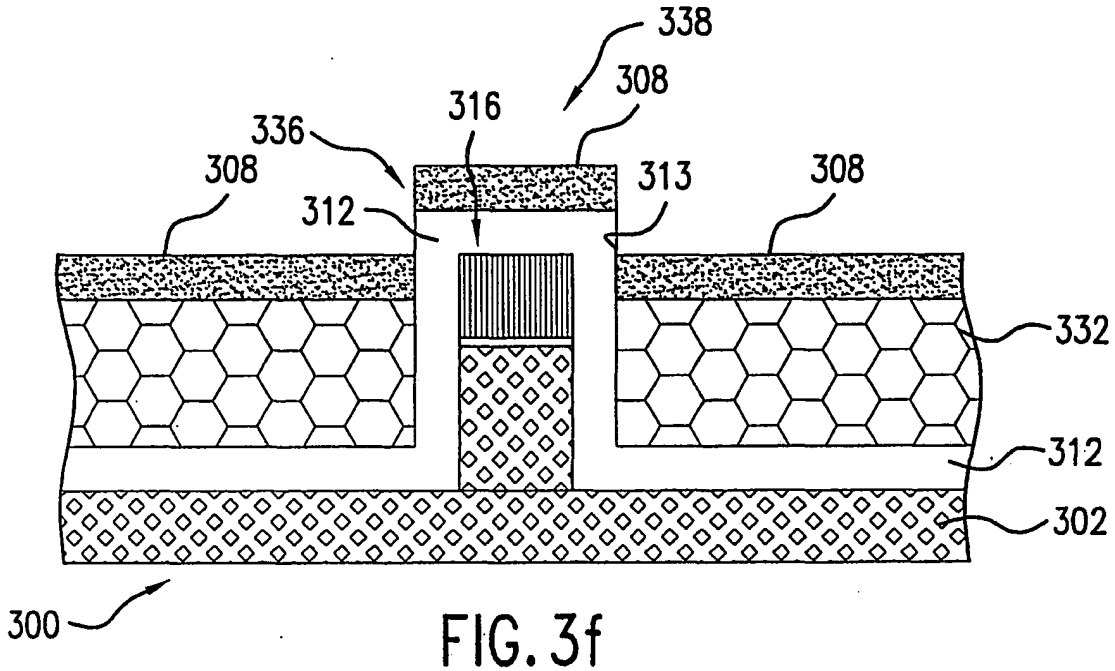


FIG. 3e


338
316
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336
308
313
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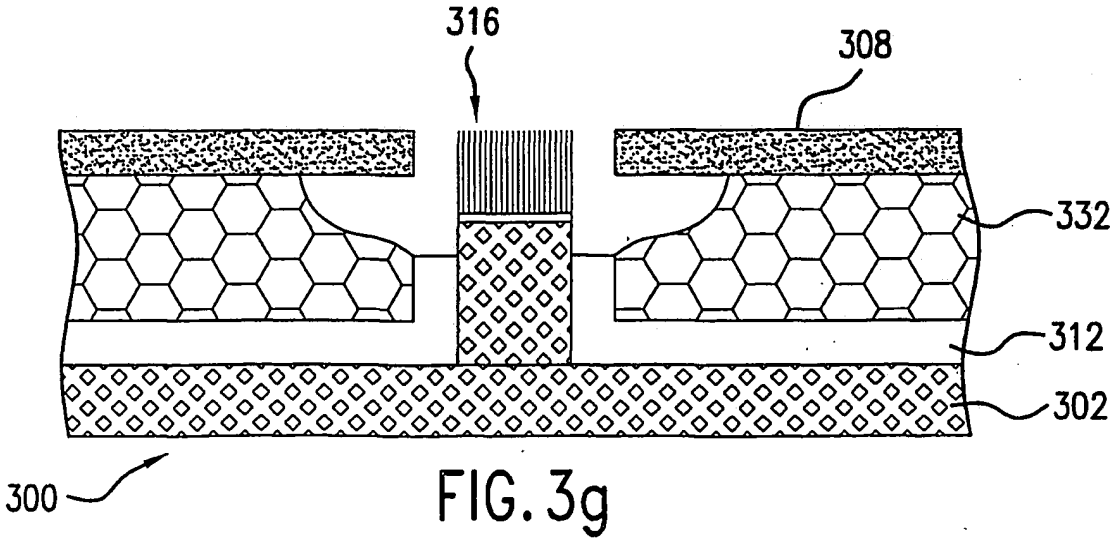
332
312
302
300

FIG. 3f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332
312
302
300

FIG. 3g

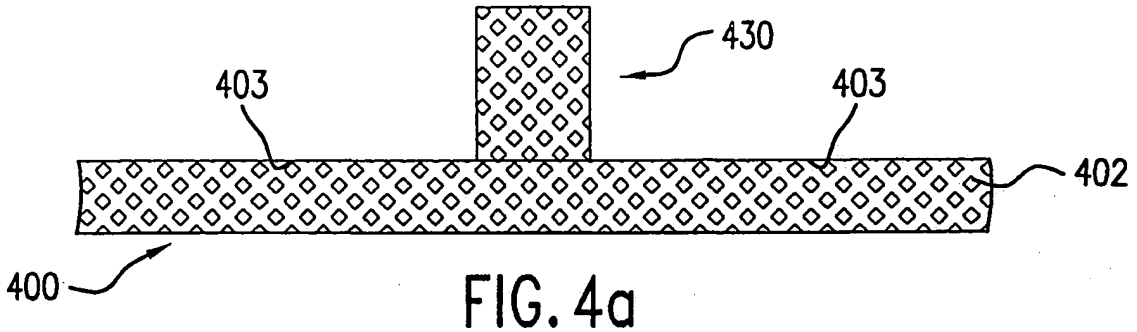


FIG. 4a

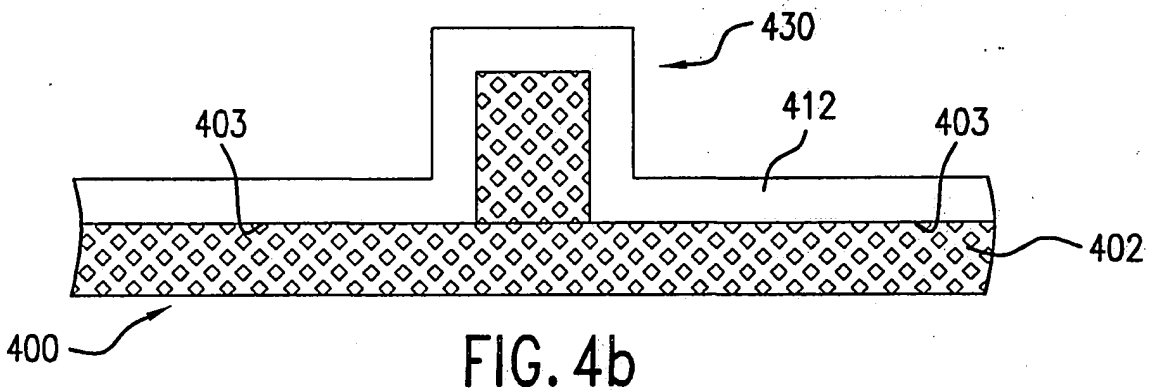


FIG. 4b

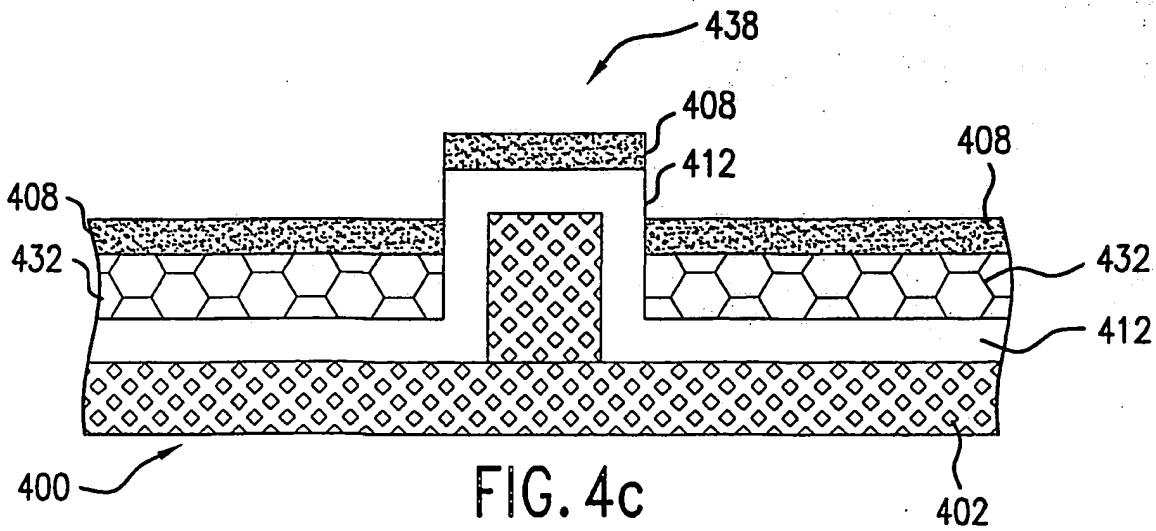


FIG. 4c

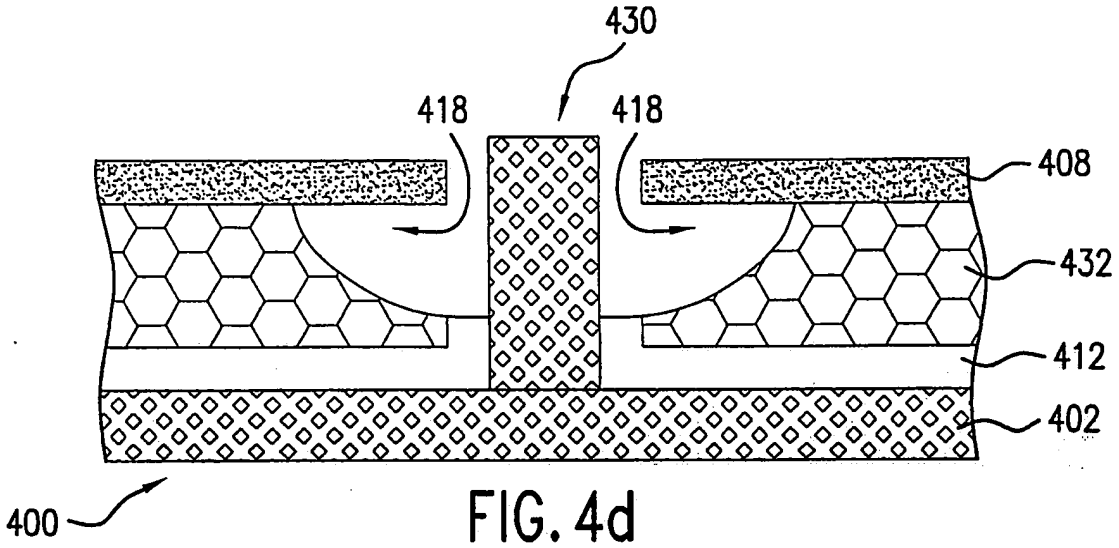


FIG. 4d

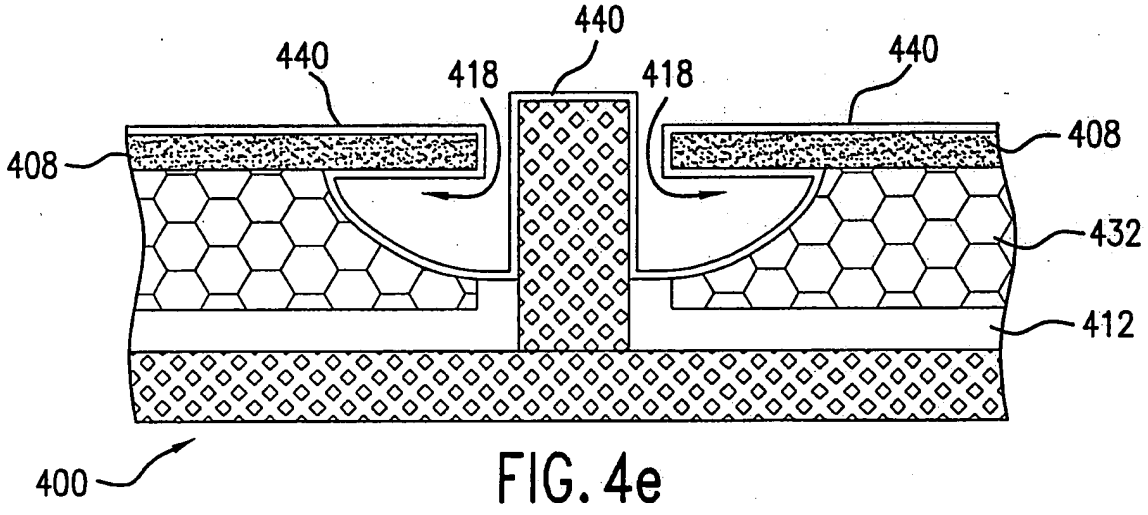


FIG. 4e

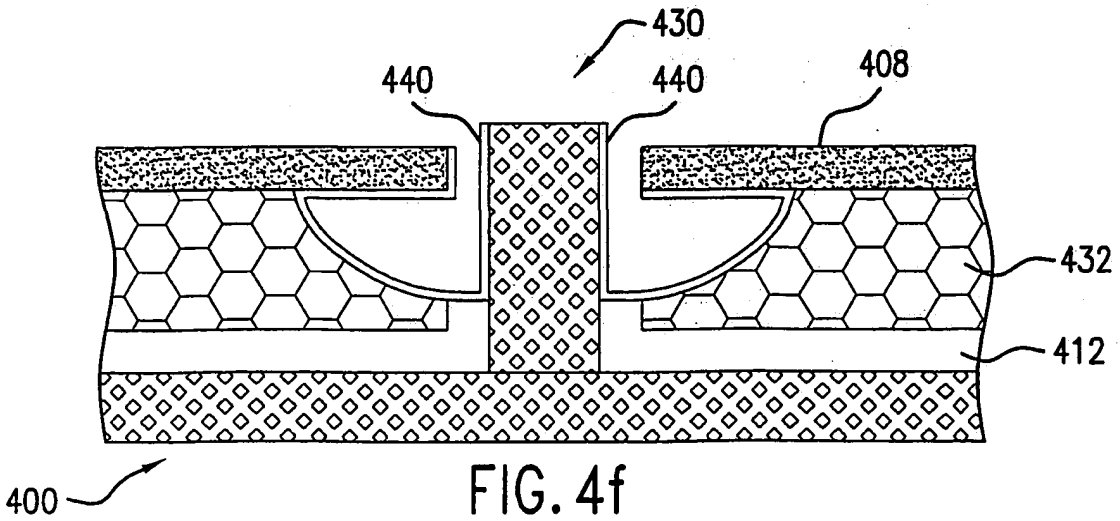
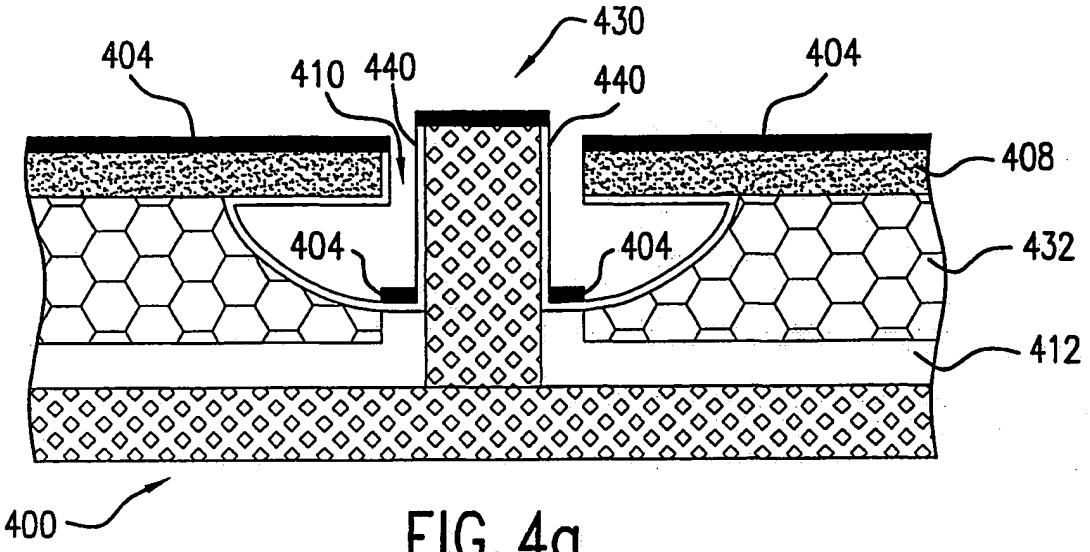


FIG. 4f


430
404
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404
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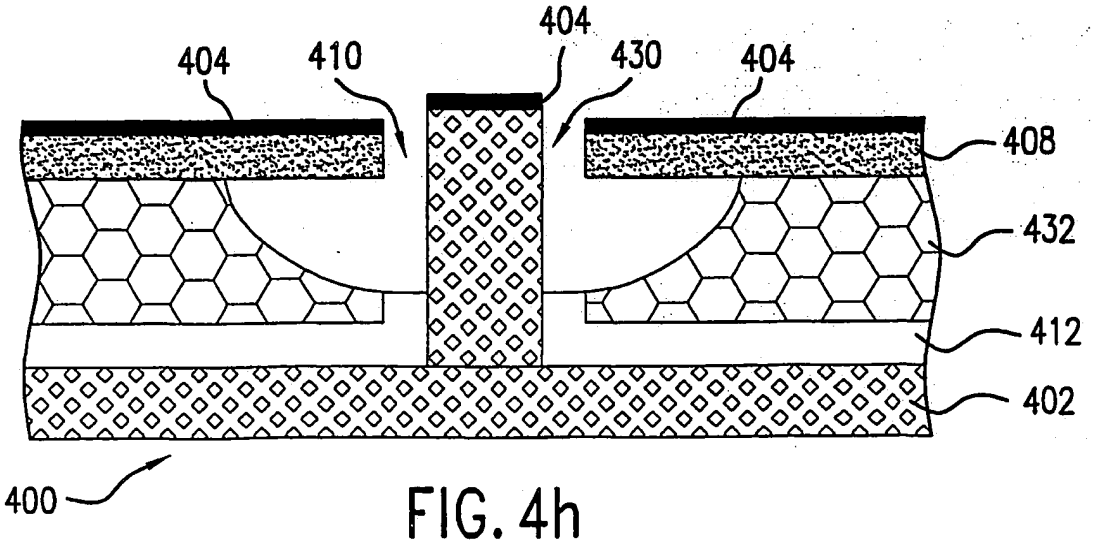
432
412
400

FIG. 4g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400

FIG. 4h

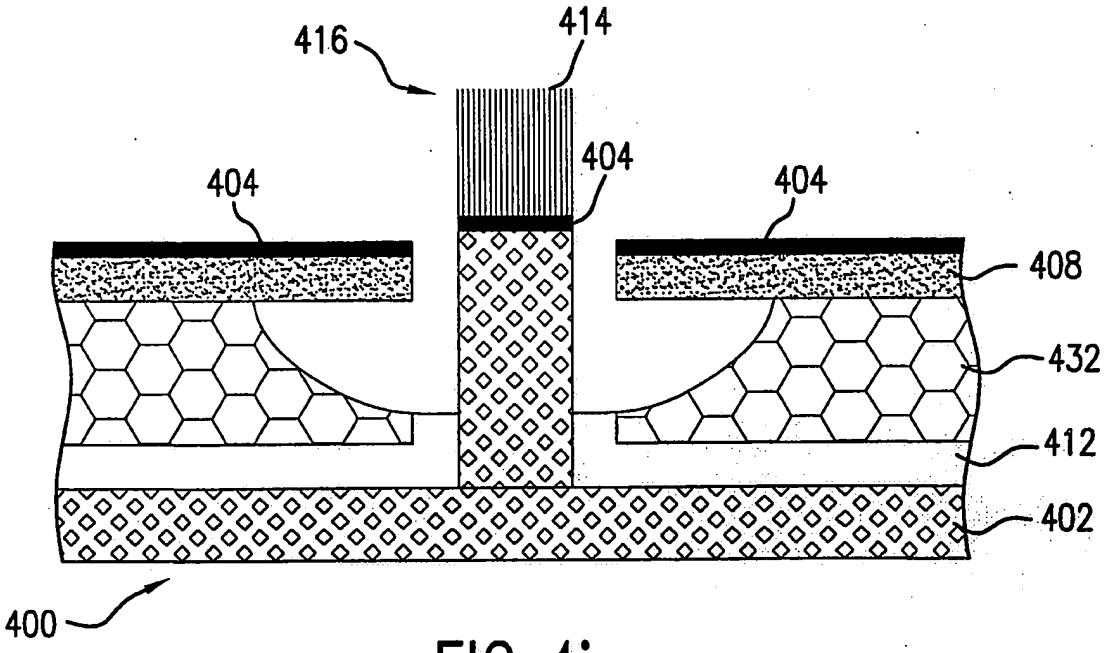


FIG. 4i

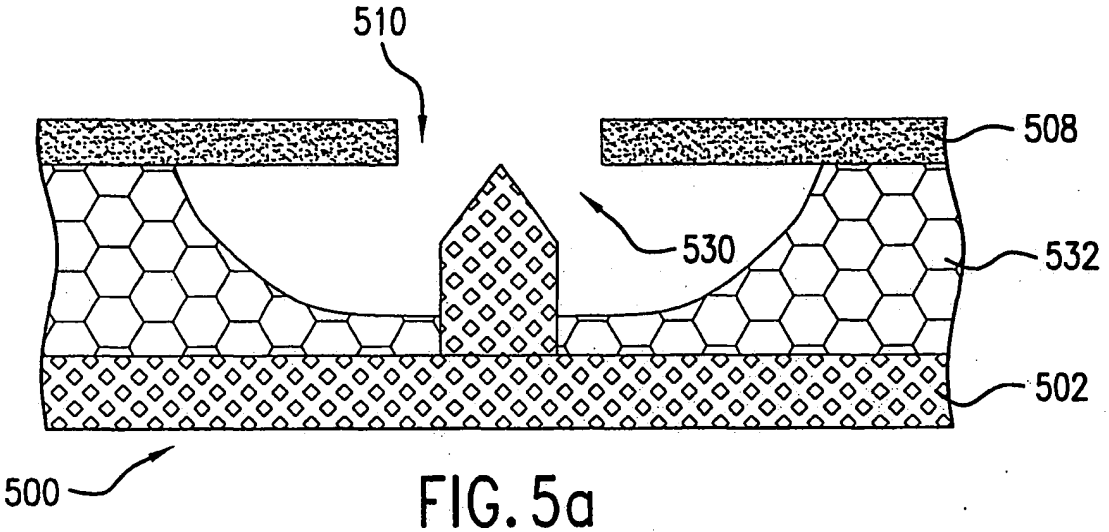


FIG. 5a

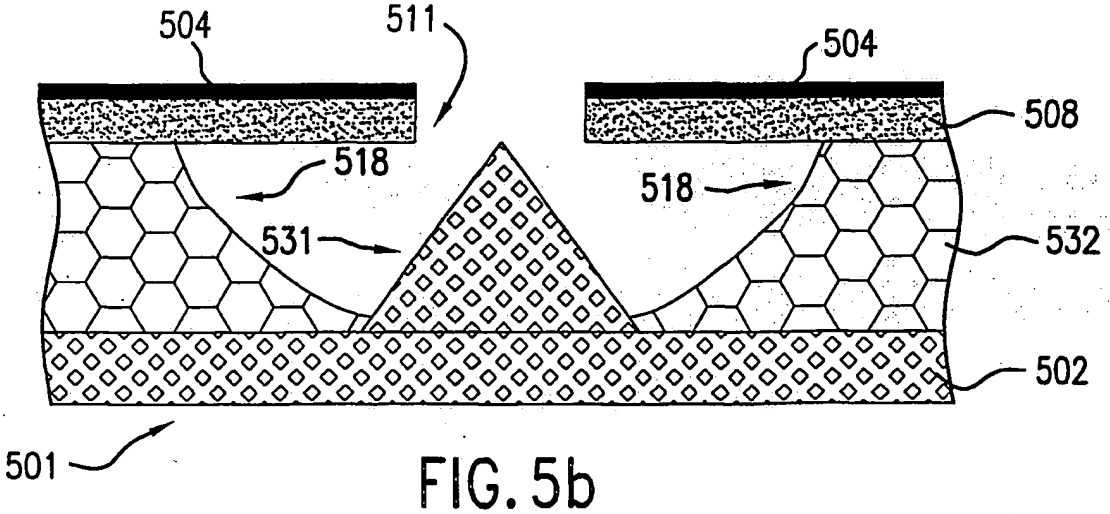
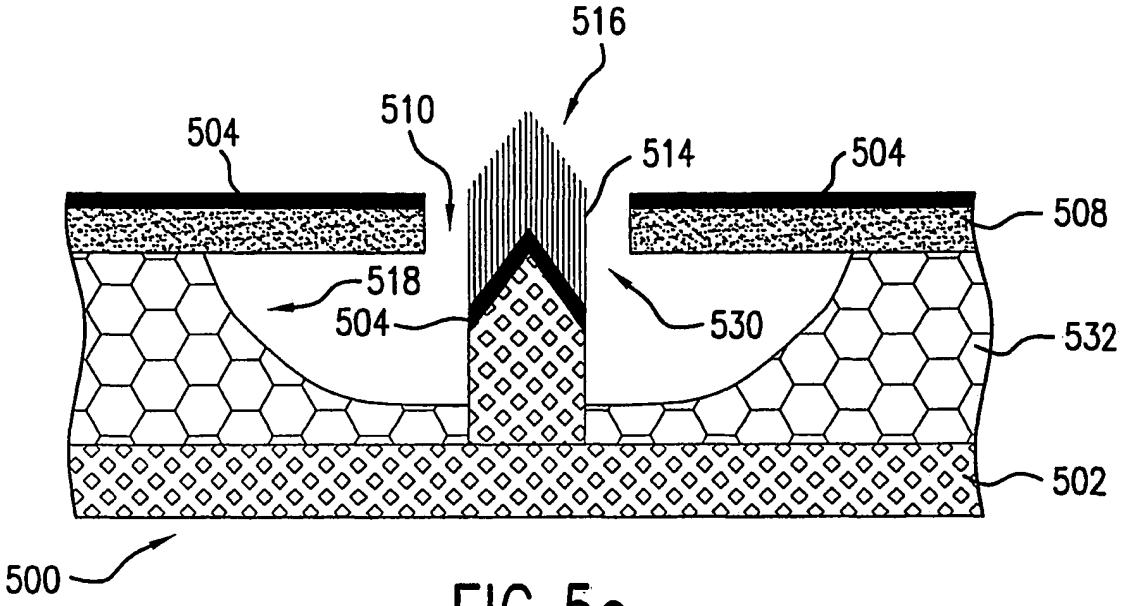


FIG. 5b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514
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518
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FIG. 5c

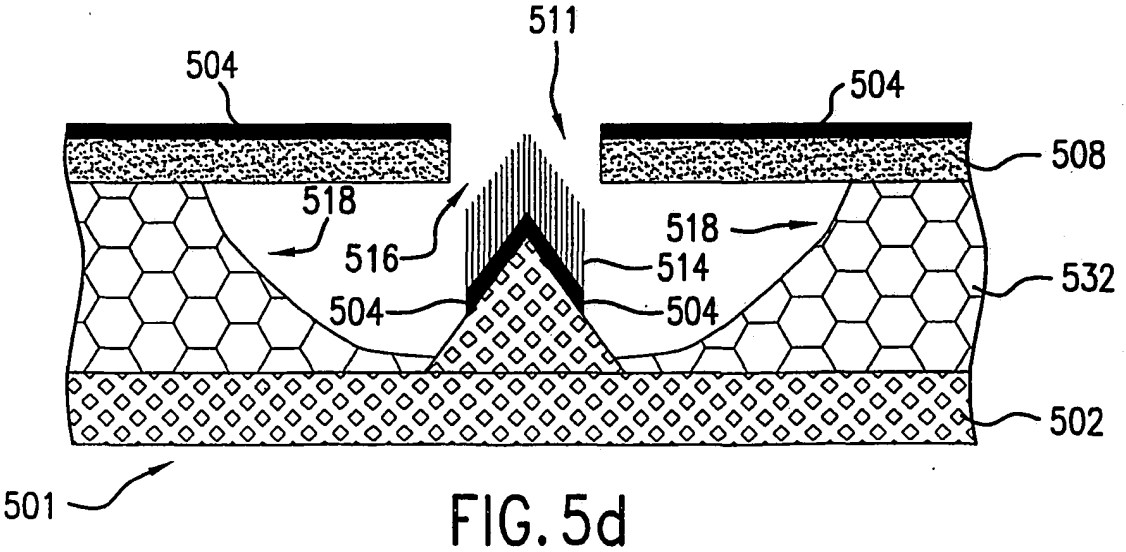
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FIG. 5d

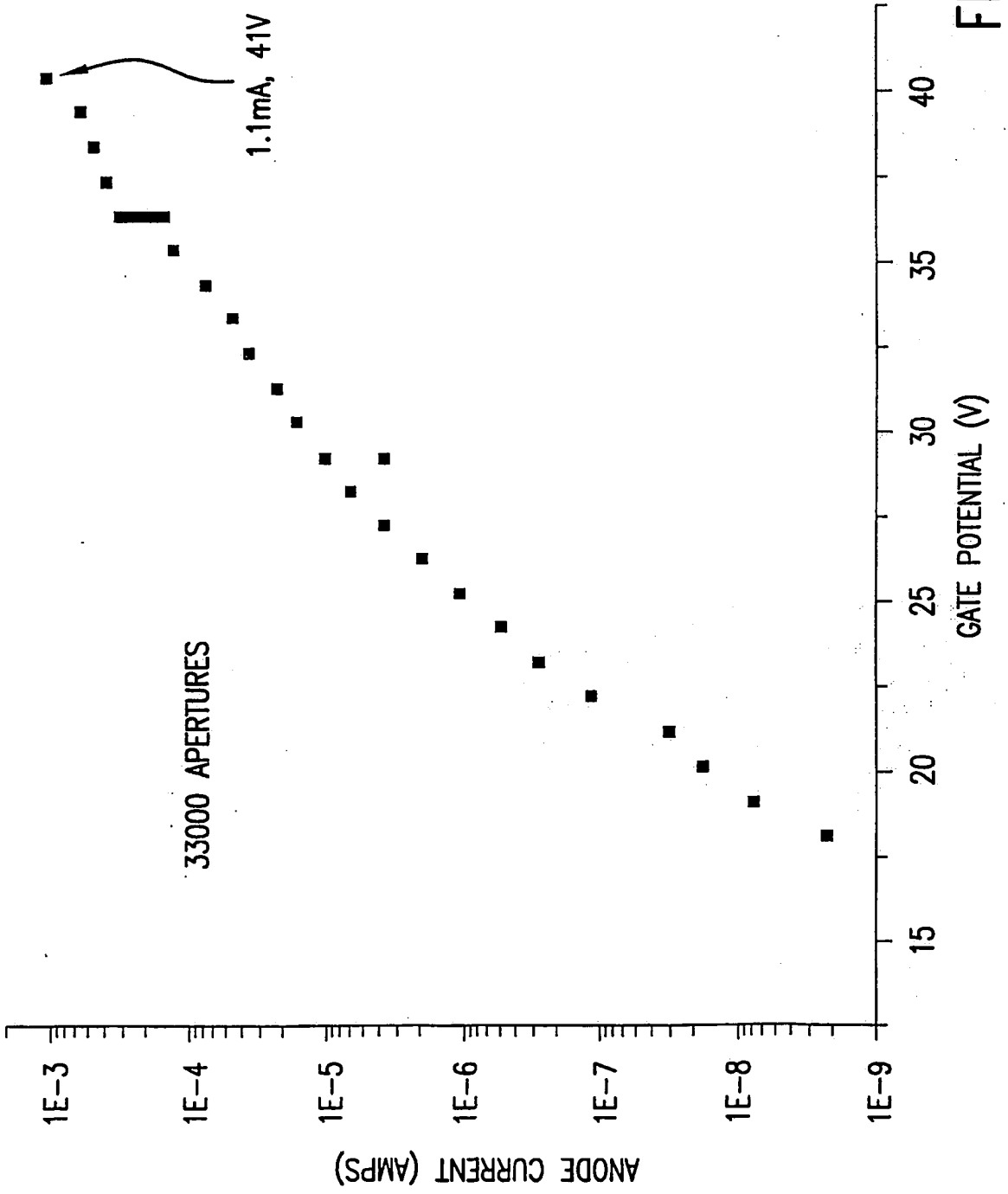

1.1mA, 41V
33000 APERTURES
ANODE CURRENT (AMPS)
1E-3
1E-4
1E-5
1E-6
1E-7
1E-8
1E-9
15
20
25
30
35
40
GATE POTENTIAL (V)

FIG. 5e

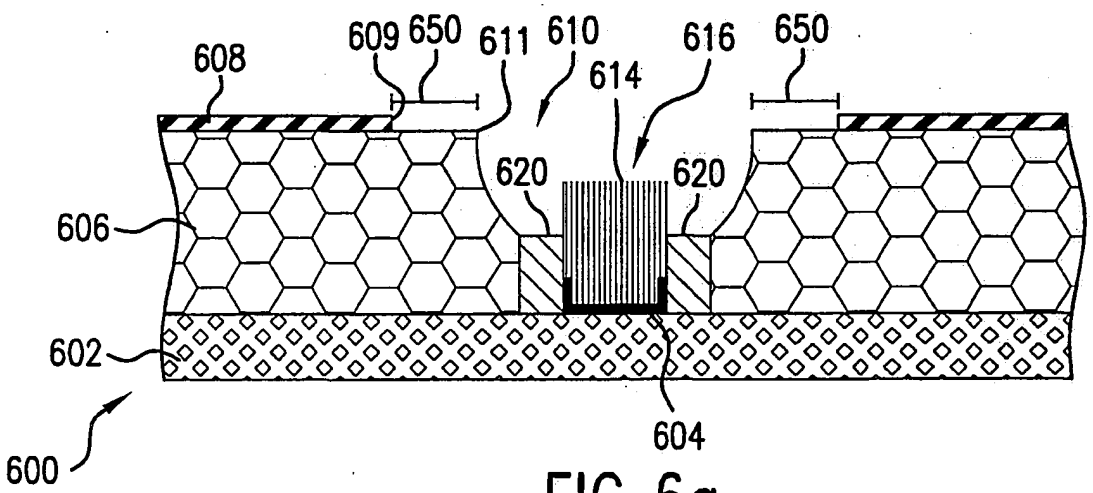


FIG. 6a

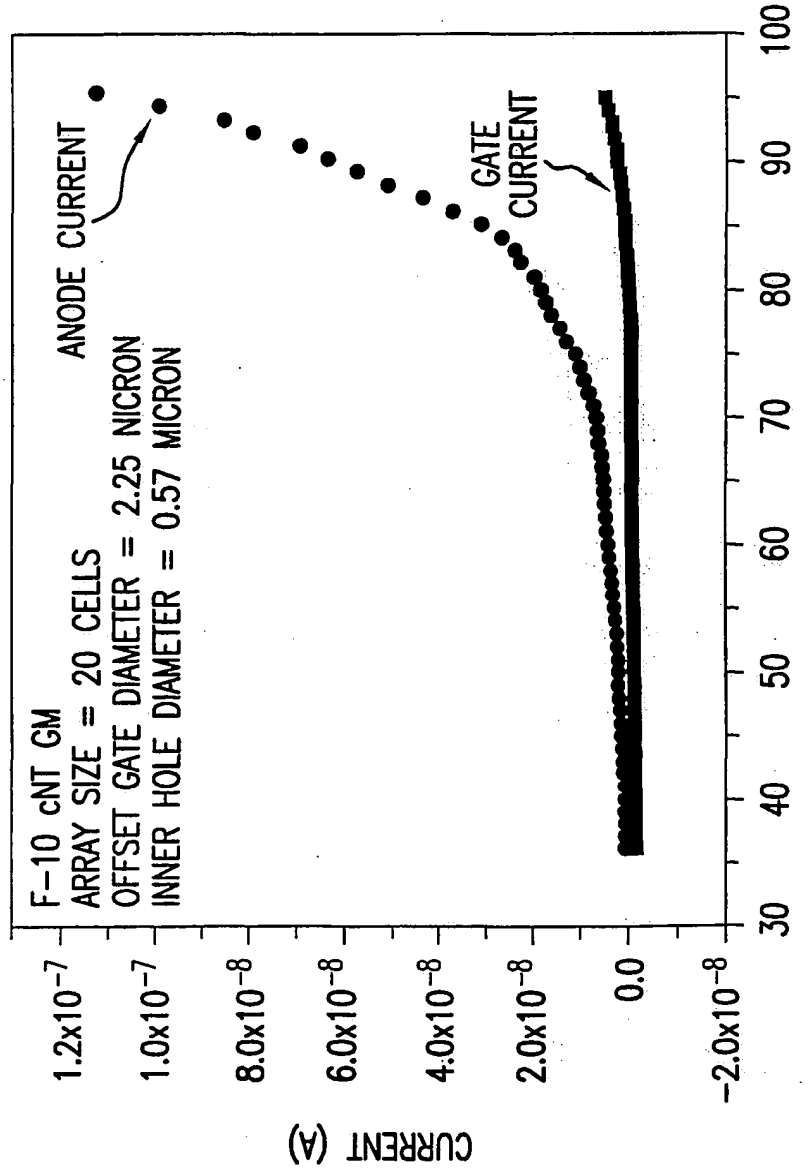

F-10 cNT GM
ARRAY SIZE = 20 CELLS
OFFSET GATE DIAMETER = 2.25 NICRON
INNER HOLE DIAMETER = 0.57 MICRON
ANODE CURRENT
GATE CURRENT
CURRENT (A)
1.2x10⁻⁷
1.0x10⁻⁷
8.0x10⁻⁸
6.0x10⁻⁸
4.0x10⁻⁸
2.0x10⁻⁸
0.0
-2.0x10⁻⁸
30
40
50
60
70
80
90
100
GATE VOLTAGE (V)

FIG. 6b

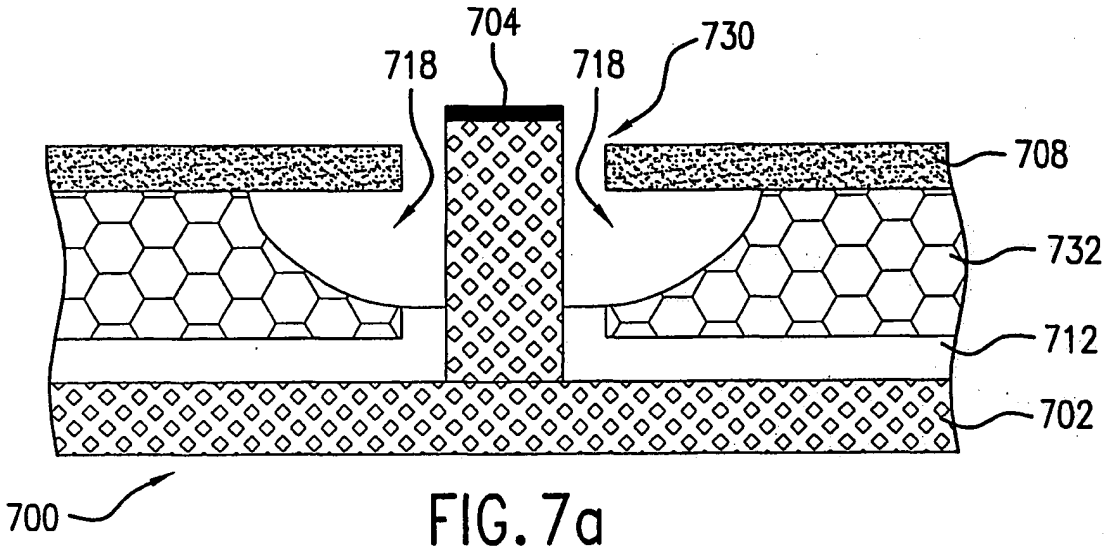
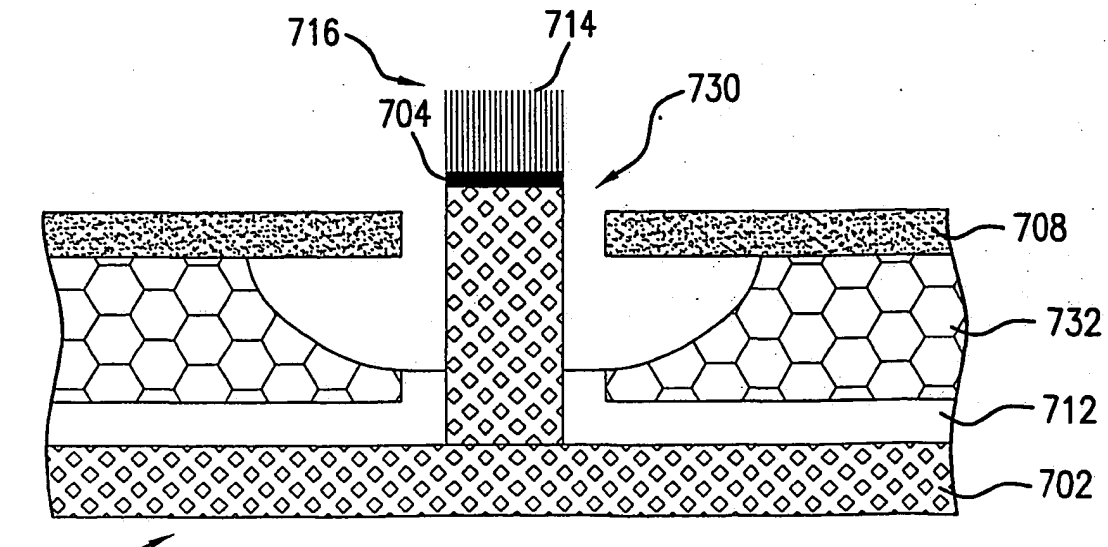

704
718
718
730
708
732
712
702
700

FIG. 7a


716
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704
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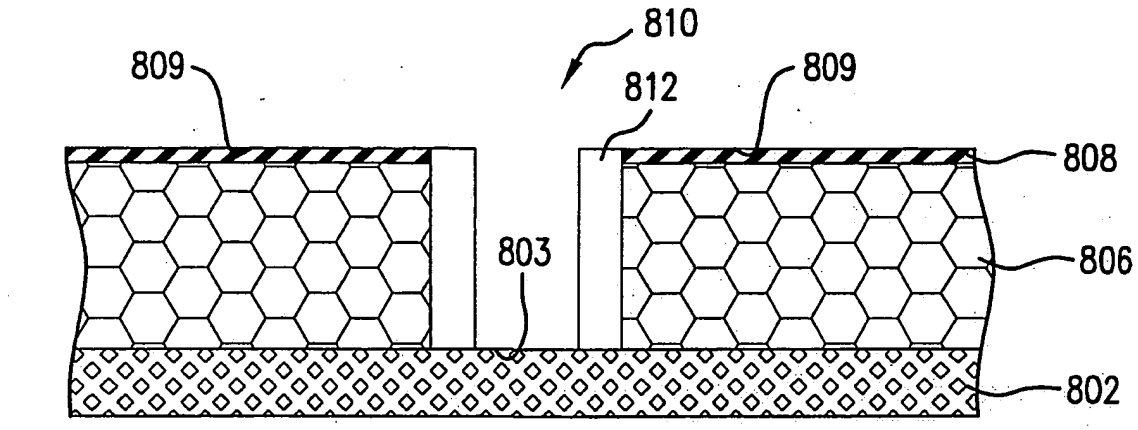
732
712
702
700

FIG. 7b


810
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812
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808
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802
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FIG. 8a

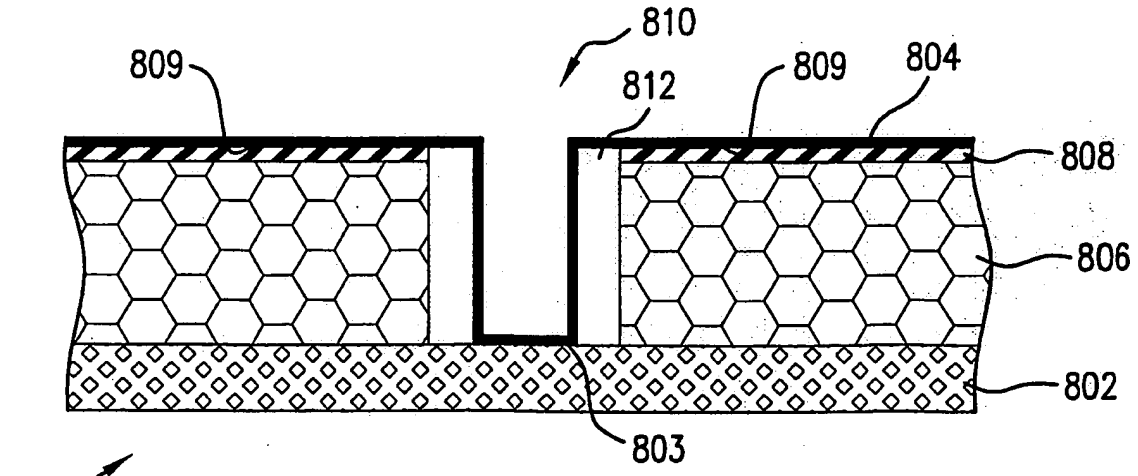
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FIG. 8b

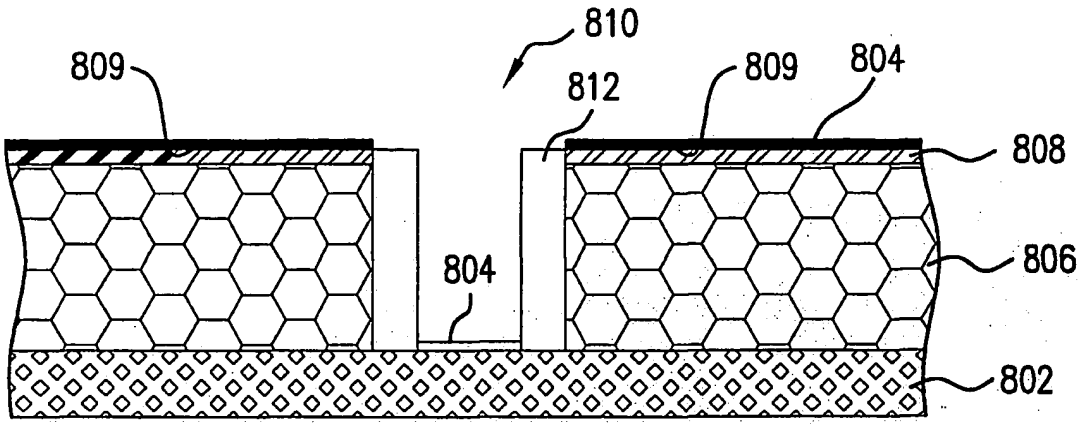
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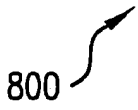
FIG. 8c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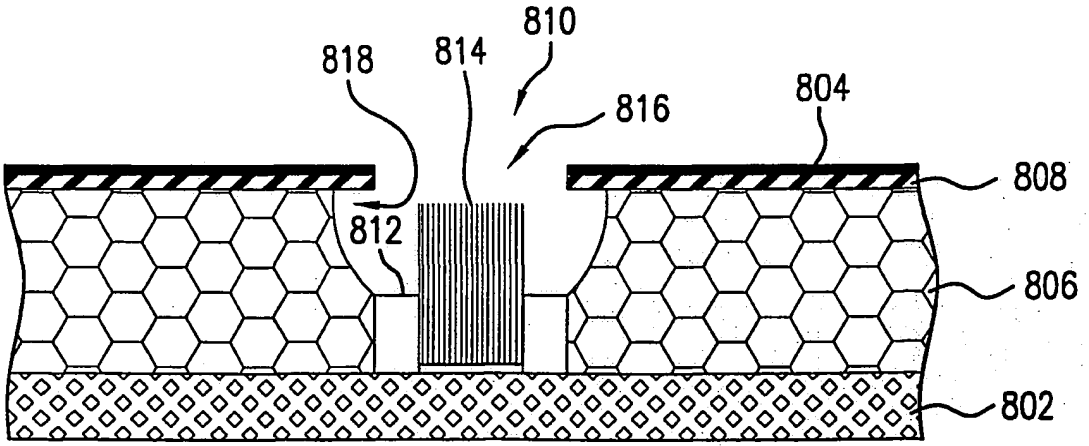
818
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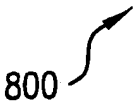
FIG. 8d


800

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US01/32572

A. CLASSIFICATION OF SUBJECT MATTER

IPC(7) :H01L 21/00
US CL :438/20; 445/46, 49, 50, 51
According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

U.S. : 438/20; 445/46, 49, 50, 51

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

NONE

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

USPTO APS EAST

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A,E	US 6,333,598 B1 (HSU et al) 25 December 2001 (25.12.2001), Figures.	1-50
A	US 5,973,444 A (XU et al) 26 October 1999 (26.10.1999), Figures.	1-50
A	US 5,872,422 A (XU et al) 16 February 1999 (16.02.1999), Figures.	1-50

☐ Further documents are listed in the continuation of Box C. ☐ See patent family annex.

* Special categories of cited documents:

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier document published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search

28 DECEMBER 2001

Date of mailing of the international search report

14 JAN 2002

Name and mailing address of the ISA/US
Commissioner of Patents and Trademarks
Box PCT
Washington, D.C. 20231

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Form PCT/ISA/210 (second sheet) (July 1998)*